CoreModule™ 430
(PC/104 Single Board Computer)
Reference Manual

P/N 50-1Z006-1010

Notice Page

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REVISION HISTORY

Revision	Reason for Change	Date
A, A	Initial Release	Oct/08
1.0	Added U9 chip to table 2-1; revised description of U7 chip in table 2-1; revised JP7 default to pins 2-3 in table 2-3; changed document p/n from 5001840 to 50-1Z006-1000; changed rev to 1.0	Oct/09
1010	Changed pitch of J4 header in Tables 2-2 and 3-5 to 0.079"; changed rev of this document from 1.0 to 1010; changed pin 9 in Table 3-10 from 3.6/4.0V to 3.0V max; added BIOS Setup Screens section to ch 4; replaced EOL, U14 video memory in Table 2-1 with new component; changed definition of SPI Flash device	June/12

ADLINK Technology, Incorporated
5215 Hellyer Avenue, #110
San Jose, CA 95138-1007
Tel. 408 360-0200
Fax 408 360-0222
http://www.adlinktech.com

Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLNK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

Contents

List of Figures

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Chapter 1 About This Manual

Purpose of this Manual

This manual is for designers of systems based on the CoreModule™ 430 PC/104 single board computer (SBC) module. This manual contains information that permits designers to create an embedded system based on specific design requirements.

Information provided in this reference manual includes:

- CoreModule 430 SBC Specifications
- Environmental requirements
- Major chips and features implemented
- CoreModule 430 SBC connector/pin numbers and definitions
- BIOS Setup information

Information not provided in this reference manual includes:

- Detailed chip specifications
- Internal component operation
- Standard interface pin-out tables
- Internal registers or signal operations
- Bus or signal timing for industry standard busses and signals

References

The following list of references may be helpful for you to complete your custom design successfully. Some of these references are also available on the Ampro By ADLINK web page. The web page was created for embedded system developers to share ADLINK's knowledge, insight, and expertise.

Specifications

- PC/104 Specifications Revision 2.5, November 2003

For latest revision of the PC/104 specifications, contact the PC/104 Consortium, at:

Web site: http://www.pc104.org

Major Integrated Circuit (Chip) Specifications

The following chip specifications are used in the CoreModule 430 processor module:

- DMP Electronics Inc. and the Vortex 86SX/DX CPU

  Web site: http://www.vortex86sx.com/

- Winbond Electronics and the W25Q16BV SPI Flash memory

  Web site: http://www.winbond.com/hq/enu/ProductAndSales/ProductSearch/?partno=w25q16bv

- Samsung Electronics and DDR2 on-board System Memory

  Web site: http://www.samsung.com/global/business/semiconductor/

- Hynix Semiconductor, Inc. and DDR2 on-board Video Memory

  Web site: http://www.hynix.com/gl/products/consumer/consumer_info.jsp

> **NOTE** If you are unable to locate the datasheets using the links provided, search the internet to find the manufacturer's web site and locate the documents you need.

Chapter 2 Product Overview

This introduction presents general information about the PC/104 architecture and the CoreModule 430 Single Board Computer (SBC). After reading this chapter you should understand:

- PC/104 architecture
- CoreModule 430 product description
- CoreModule 430 features
- Major components
- Header definitions
- Specifications

PC/104 Architecture

The PC/104 architecture affords a great deal of flexibility in system design. You can build a simple system using only a CoreModule Single Board Computer (SBC), with input/output devices connected to its serial or parallel ports and a Compact Flash card in the Compact Flash socket. To expand a simple CoreModule system, simply add self-stacking ADLINK MiniModules or 3rd party PC/104 expansion boards to provide additional capabilities, such as:

- Additional I/O ports
- Analog or digital I/O interfaces

PC/104 expansion modules can be stacked with the CoreModule 430 avoiding the need for card cages and backplanes. The PC/104 expansion modules can be mounted directly to the PC/104 bus connector of the CoreModule 430. PC/104-compliant modules can be stacked with an inter-board spacing of ~0.66" (16.7 mm) so that a 3-module system fits in a 3.6" x 3.8" x 2.4" space. See Figure 2-1.

One or more MiniModule products or other PC/104 modules can be installed on the CoreModule expansion connectors. When installed on the PC/104 headers, the expansion modules fit within the CoreModule outline dimensions. Most MiniModule products have stack through connectors compatible with the PC/104 Version 2.5 specification. Several modules can be stacked on the CoreModule headers. Each additional module increases the thickness of the package by 0.60" (15 mm). See Figure 2-1.

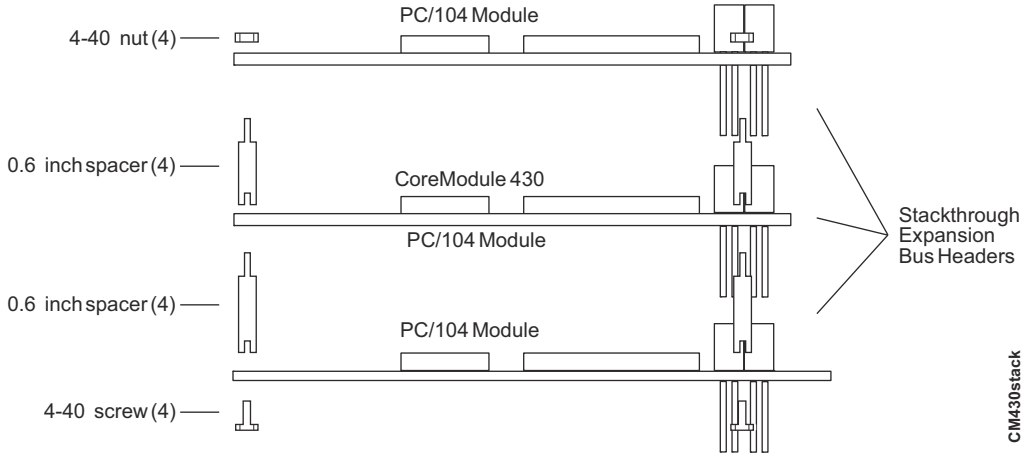

Figure 2-1. Stacking PC/104 Modules with the CoreModule 430

Product Description

The CoreModule 430 SBC is an exceptionally high integration, x86-based PC compatible system in the PC/104 form factor. This rugged and high quality single board system contains all the component subsystems of a PC/AT motherboard plus the equivalent of several PC/AT expansion boards.

In addition, the CoreModule 430 SBC includes a comprehensive set of system extensions and enhancements that are specifically designed for embedded systems. These enhancements ensure fail-safe embedded system operation, such as a watchdog timer. The CoreModule 430 is designed to meet the size, power consumption, temperature range, quality, and reliability demands of embedded applications. The CoreModule 430 requires a single +5V power source.

The CoreModule 430 SBC is particularly well suited to either embedded or portable applications. Its flexibility makes system design quick and easy. It can be stacked with ADLINK MiniModules or other PC/104-compliant expansion boards, or it can be used as the computing engine in a fully customized application.

Module Features

- CPU
  - Provides x86 based DMP Vortex SX (300 MHz) or DX (800 MHz) microprocessor
  - Provides integrated Northbridge and Southbridge
  - Fully supports PC compatible architecture
  - Provides 8 kB Unified Instruction and Data Cache
  - Provides Parallel Processing Integrated Floating Point Unit (only in DX version)
  - Provides Low Power and System Management Modes
- Memory
  - Provides up to 256 MB standard DDR2 system RAM (soldered on the board)
  - Provides up to 32 MB standard DDR2 video RAM (soldered on the board)
  - Supports Memory Bus Speeds of 166 MHz on the SX CPU and 333 MHz on the DX CPU
- PC/104 Bus Interface
  - Provides standard PC/104 connector
  - Supports clock speeds up to 8 MHz ISA
- IDE Interface
  - Provides one IDE channel
  - Supports two enhanced IDE devices
  - Provides Fast ATA-capable interface for high-speed PIO modes (PIO modes 0 to 4)
  - Supports ATAPI and DVD peripherals
  - Supports IDE native and ATA compatibility modes
- Compact Flash Socket
  - Provides Compact Flash socket (Type I or II)
  - Supports IDE Compact Flash cards
  - Attached to Primary IDE bus

- Serial Ports
  - Provides two 10-pin headers and four buffered RS-232 serial ports with full handshaking and modem capability
  - Provides 16C550 or 16C552 UARTs, each with a built-in 16-byte FIFO buffer
  - Supports RS-232 or RS-485 operation on ports 1 and 2
  - Supports programmable word length, stop bits, and parity
  - Supports 16-bit programmable baud-rate generator and an interrupt generator
- Parallel Port (LPT)
  - Provides parallel port header
  - Supports standard printer port
  - Supports IEEE standard 1284 protocols, including SPP, EPP, and ECP modes
  - Supports 16 byte FIFO for ECP mode
- Ethernet
  - Supports IEEE 802.3 10BaseT/100BaseT compatible physical layer
  - Supports Auto-negotiation for speed, duplex mode, and flow control
  - Supports full duplex or half-duplex mode
    - Full-duplex mode supports transmit and receive frames simultaneously
    - Supports IEEE 802.3x Flow control in full duplex mode
    - Half-duplex mode supports enhanced proprietary collision reduction mode
- Utility Interface
  - PS/2 Keyboard and Mouse Interface
  - Supports external battery for Real Time Clock operation
  - Supports standard external 8Ω speaker interface
  - Supports external reset switch
- USB Ports
  - Provides one root USB hub
  - Provides two USB ports
  - Supports USB v2.0 and Universal UHCI v1.1
- Video (TTL/VGA) Display

  Enhanced 2D graphics controller
  - Supports BitBLT implementation for all 256 raster operations for Windows® support
  - Provides hardware command queue
  - Supports all BLT transparency modes
    - Bitmap transparency
    - Pattern transparency
    - Source transparency
    - Destination transparency
  - Supports rectangle clipping
  - Supports fast line draw engine with styled pattern

- Supports fast rectangle fill engine
- Supports 64x64x2 bit-mapped mono hardware cursor
- Supports 256MB frame buffer with linear addressing

VGA Interface (DB15)

- VGA Controller with 135 MHz triple RAMDACs for 1280 x 1024 x 75 Hz display
- Supports 24-bit pixel depth
- Interlaced or non-interlaced output

TTL Interface

- Supports VESA Flat Panel Display interface
- Supports programmable panel size up to 1600x1200 pixel display resolution
- Supports internal CRT controller for display mode settings
- Supports 12-, 18-, and dual 12-bit interface (1 Pixel/Clock)
- Supports 3.3V or 5V LCD panels; jumper selectable

- Miscellaneous
  - Provides Real Time Clock and CMOS RAM, with support for battery-free operation
  - Provides General Purpose I/O (GPIO) interface
  - Supports Oops! Jumper (BIOS Recovery)
  - Supports Remote Access (Console Redirection)
  - Supports customizable Splash Screen
  - Supports Watchdog Timer (WDT)
  - Provides 16 Mbits of virtual floppy drive capacity

Block Diagram

Figure 2-2 shows the functional components of the module.

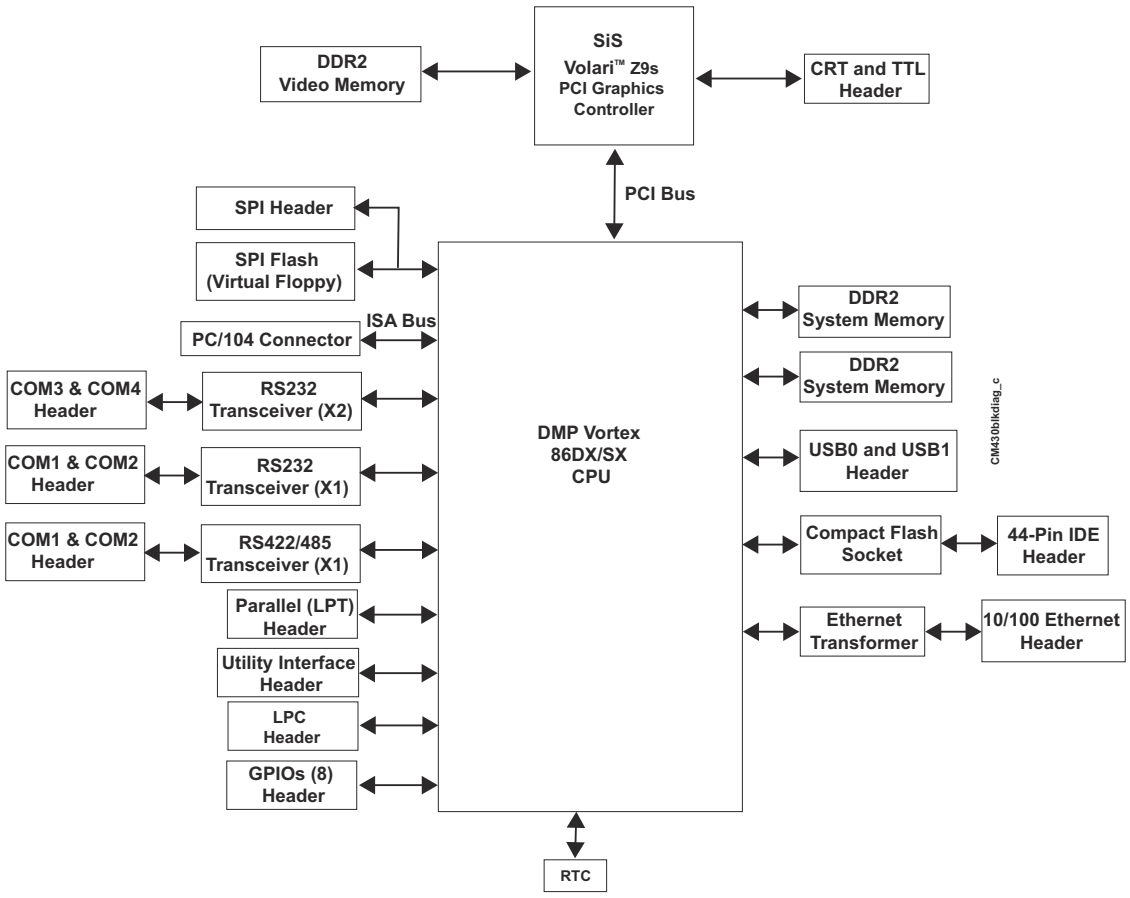

Figure 2-2. Block Diagram

Major Components (ICs)

Table 2-1 describes the major integrated circuits (ICs) on the CoreModule 430, and Figure 2-3 shows the locations of the major ICs on the board.

Table 2-1. Major Components (Chips) Descriptions and Functions

Chip Type	Mfg.	Model	Description	Function
CPU (U1)	DMP Electronics, Inc.	Vortex 86SX/DX	x86 32-bit processor	Integrates Processor Core, Memory Controller, and I/O Hub
PCI Graphics Controller (U13)	SiS Corporation	Volari Z9S	PCI graphics controller	Integrates 2D Engine and PCI controller
DDR2 System Memory (U2 and U3)	Fluctuating	Fluctuating	On-board DDR2 128Mx8 System memory	Provides high-speed data transfer
DDR2 Video Memory (U14)	Fluctuating	Fluctuating	On-board DDR2 32Mx16 Video memory	Provides high-speed data transfer
RS232 Transceiver (U4 - on back of the board)	Analog Devices	ADM213EARSZ	RS232 Transceiver for COM3	Transmits and receives RS232 signals for COM3
RS232 Transceiver (U5)	Analog Devices	ADM213EARSZ	RS232 Transceiver for COM4	Transmits and receives RS232 signals for COM4
SPI Flash (U6)	Winbond	W25Q16BV	Serial Peripheral Interface 16 Mbit Flash Memory	Stores data in flash memory, emulating a floppy drive
RS232 Transceiver (U7)	Analog Devices	ADM213EARSZ	RS232 Transceiver for COM1 and COM2	Transmits and receives RS232 signals for COM1 and COM2
RS422/485 Transceiver (U9 - on back of the board)	Linear	LTC1334CG#PBF	RS422/485 Transceiver for COM1 and COM2	Transmits and receives RS422/485 signals for COM1 and COM2
Ethernet Transfomer (U12)	Pulse	H1102NL-T	10/100BaseT Ethernet Magnetics	Provides electrical isolation for Ethernet controller contained in the CPU

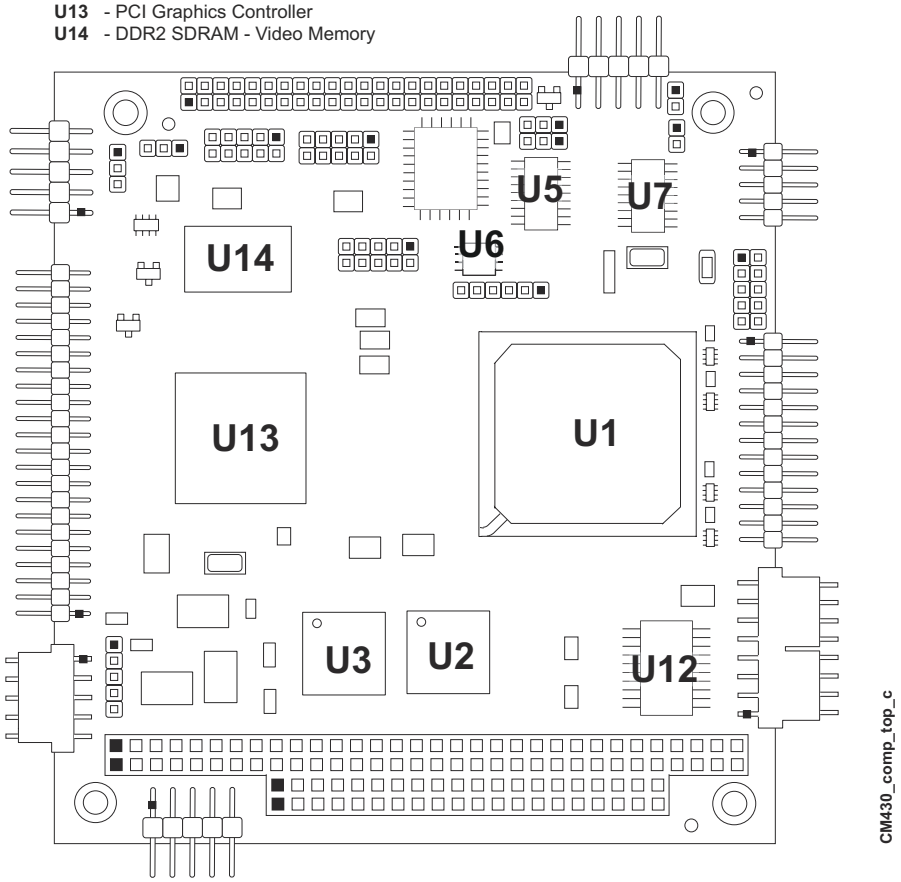

Figure 2-3. Component Locations (Top Side)

NOTE	Pin 1 is shown as a black pin (square or round) on vertical headers or connectors in all illustrations. Black dots on right-angle headers or connectors indicate pin 2.

Header, Connector, and Socket Definitions

Table 2-2 describes the headers shown in Figure 2-5.

Table 2-2. Header, Connector, and Socket Descriptions

Jack/Plug #	Access	Description
P1A/1B & P1C/1D – PC/104 Bus	Top/ Bottom	104-pin, 0.100" (2.54mm) connectors for PC/104 (ISA) bus
J2 – Ethernet	Top	8-pin, 0.100" (2.54mm), right-angle header for Ethernet interface
J3 – Serial 1 (COM1)	Top	10-pin, 0.100" (2.54mm), right-angle header for Serial 1 interface
J4 – Parallel (LPT)	Top	26-pin, 0.079" (2mm), right-angle header for Parallel interface
J5 – Utility	Top	10-pin, 0.100" (2.54mm), right-angle header for Utility interface
J6 – IDE	Top	44-pin, 0.079" (2mm) header for IDE interface
J7 – Power	Top	10-pin, 0.100" (2.54mm), right-angle header for Power connection
J8 – GPIO (User)	Top	10-pin, 0.079" (2mm) header for User defined GPIO signals
J9 – Serial 2 (COM2)	Top	10-pin, 0.100" (2.54mm), right-angle header for Serial 2 interface
J10 – USB0	Top	5-pin, 0.100" (2.54mm), right-angle header for USB0 interface
J11 – Video	Top	44-pin, 0.079" (2mm), right-angle header for LCD/CRT interface
J12 – Compact Flash	Bottom	50-pin, 0.050" (1.27mm) socket for Type I or II Compact Flash cards
J13 – Serial 4 (COM4)	Top	10-pin, 0.100" (2.54mm) header for Serial 4 interface
J14 – Serial 3 (COM3)	Top	10-pin, 0.100" (2.54mm) header for Serial 3 interface
J15 – DNP	Top	Do not populate
J17 – USB1	Top	5-pin, 0.079" (2mm) header for USB1 interface
J19 – SPI	Top	6-pin, 0.100" (2.54mm) header used for SPI Flash programming
J20 – LPC	Top	10-pin, 0.079" (2mm) header for LPC signals

NOTE The pinout tables in Chapter 3 of this manual identify pin sequence using the following methods: A 10-pin header with two rows of pins, using odd/even numbering, where pin 2 is directly across from pin 1, is noted as 10-pin, 2 rows, odd/even (1, 2). Alternately, a 20-pin connector using consecutive numbering, where pin 11 is directly across from pin 1, is noted in this way: 20-pin, 2 rows, consecutive (1, 11). The second number in the parenthesis is always directly across from pin 1. See Figure 2-4.

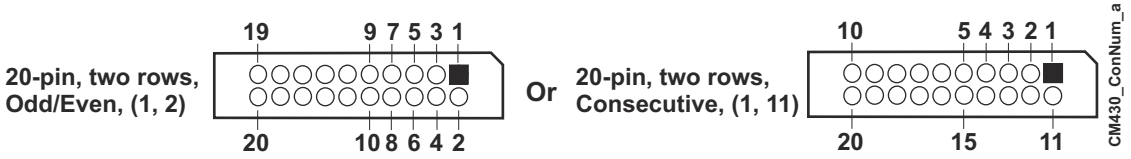

Figure 2-4. Connector Pin Identifications

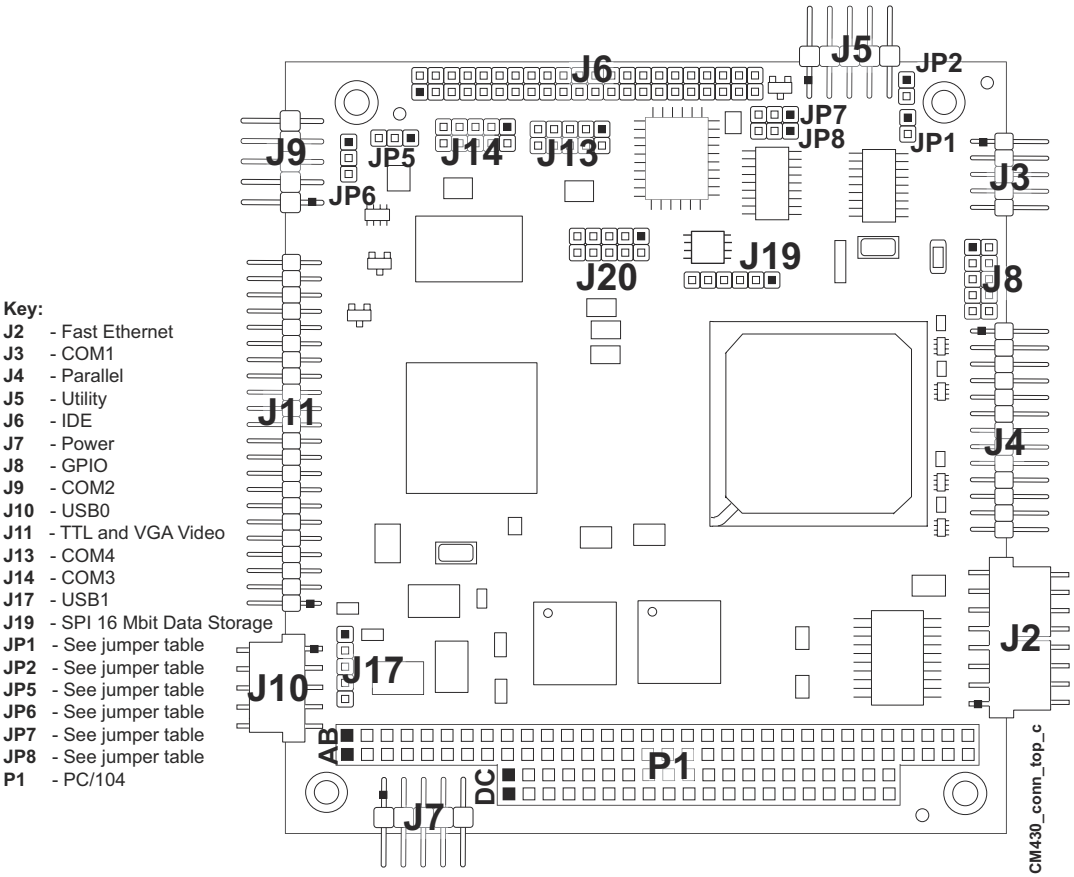

Figure 2-5. Header Locations (Top Side)

Jumper Header Definitions

Table 2-3 describes the jumper headers shown in Figure 2-5.

Table 2-3. Jumper Settings

Jumper #	Installed	Removed/Installed
JP1 – Serial Port 2 Termination	Enable RS-485 Termination (Pins 1-2)	Disable RS-485 Termination (Removed) **Default** setting
JP2 – Serial Port 1 Termination	Enable RS-485 Termination (Pins 1-2)	Disable RS-485 Termination (Removed) **Default** setting
JP5 – Backlight Voltage Select	+5 Volts (Pins 1-2)	+12 Volts (Pins 2-3) **Default**
JP6 – Flat Panel Voltage Select	+3.3 Volts (Pins 1-2) **Default**	+5 Volts (Pins 2-3)
JP7 – Compact Flash Voltage Select	+5 Volts (Pins 1-2)	+3.3 Volts (Pins 2-3) **Default**
JP8 – IDE Select	Enable HDD master, CF slave (Pins 1-2) **Default**	Enable HDD slave, CF master (Pins 2-3)

Note: All jumper headers use 0.079" (2mm) pitch.

Specifications

Physical Specifications

Table 2-4 shows the physical dimensions of the module and Figure 2-6 shows the mounting dimensions.

Table 2-4. Weight and Footprint Dimensions

Item	Dimension
Weight	0.10 kg. (0.20 lbs.)
Height (upper surface)	10.99mm (0.43") See Note on page 13.
Width	90.2mm (3.6")
Length	95.9mm (3.8")

NOTE Height is measured from the upper board surface to the highest permanent component (PC/104 connector) on the upper board surface. This does not include the heatsink.

Mechanical Specifications

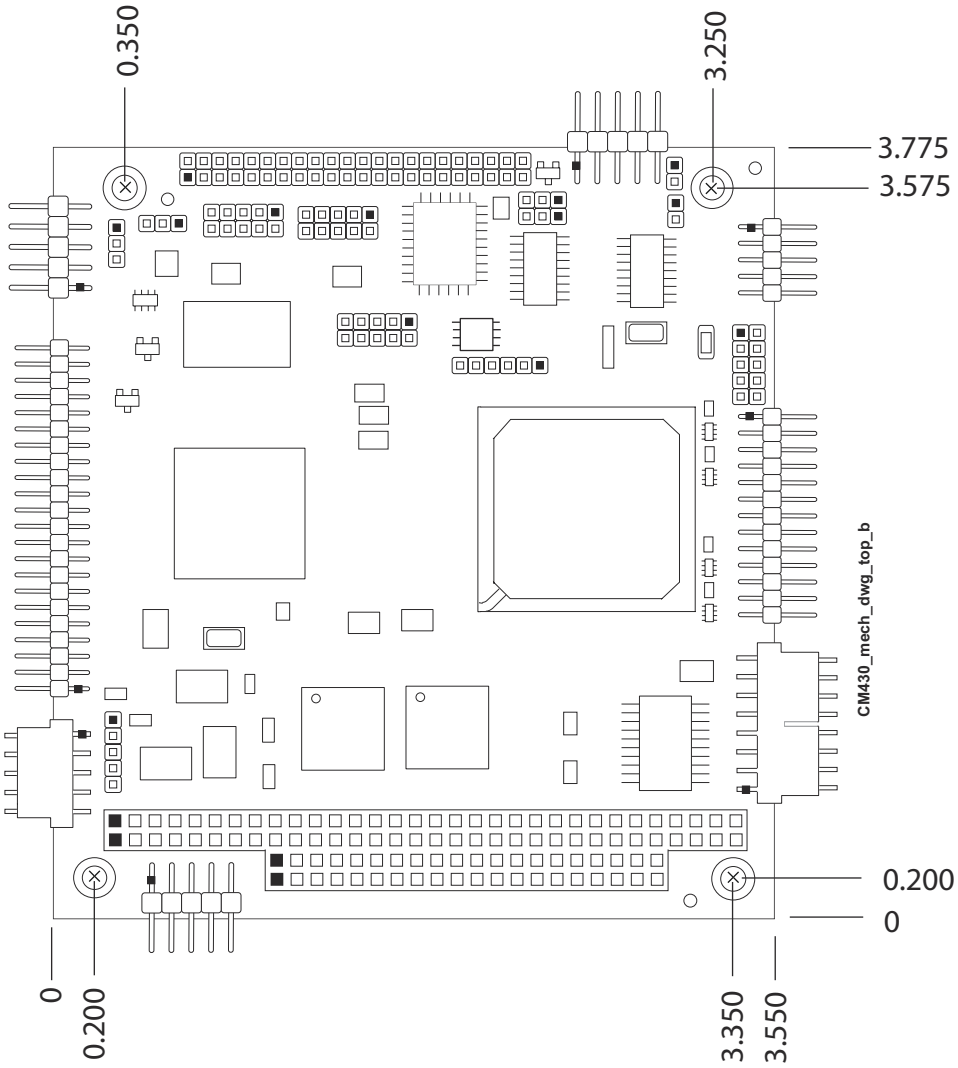

Figure 2-6. Mechanical Dimensions (Top Side)

> **NOTE** All dimensions are given in inches. Pin 1 is shown as a black pin (square or round) on vertical headers or connectors in all illustrations. Black dots on right-angle headers or connectors indicate pin 2.
>
> The Compact Flash socket (J12) exceeds the PC/104 height limitation by 0.2 inches.

Power Specifications

Table 2-5 provides the power requirements for the 300 MHz and 800 MHz versions of the CoreModule 430.

Table 2-5. Power Supply Requirements

Parameter	Characteristics for 300 MHz CPU	Characteristics for 800 MHz CPU
Input Type	Regulated DC voltages	Regulated DC voltages
Peak In-rush Current	14.80A (74.00W)	14.86A (74.30W)
Idle Current	1.30A (6.51W)	1.42A (7.12W)
BIT Current (Typical)	1.32A (6.58W)	1.44A (7.19W)

Operating configurations:

- In-rush operating configuration includes CRT video, 256MB DDR RAM, and power.
- Idle operating configuration includes the in-rush configuration as well as on-board Compact Flash with 64MB card, and one keyboard.
- BIT = Burn-In-Test. Operating configuration includes idle configuration as well as two serial port loop-backs, one Ethernet connection, and four USB Compact Flash readers with 64MB Compact Flash.

Environmental Specifications

Table 2-6 provides the operating and storage condition ranges required for this module.

Table 2-6. Environmental Requirements

Parameter	Conditions
Temperature	
Operating	–20° to +70° C (–4° to +158° F)
Extended (Optional)	–40° to +85° C (–40° to +185° F)
Storage	–55° to +85° C (–67° to +185° F)
Humidity	
Operating	5% to 90% relative humidity, non-condensing
Non-operating	5% to 95% relative humidity, non-condensing

Thermal/Cooling Requirements

The CPU is the primary source of heat on the board. The 800 MHz version of the CoreModule 430 CPU is designed to operate at its maximum speed and requires a heatsink (provided). The 300 MHz version of the CoreModule 430 CPU does not require a heatsink.

Chapter 3 Hardware

Overview

This chapter discusses the chips and connectors of the module features in the following order:

- CPU
- Graphics
- Memory
  - System Memory
  - Video Memory
  - SPI Flash
- Memory Map
- Interrupt Channel Assignments
- I/O Address Map
- Serial
- Parallel (LPT)
- Utility
  - Keyboard
  - Mouse
  - Battery
  - Reset Switch
  - Speaker
- Ethernet
- USB
- Video
- SPI
- LPC
- Miscellaneous
  - Time of Day/RTC
  - User GPIO
  - Oops! Jumper (BIOS Recovery)
  - Watchdog timer
- Power

> **NOTE** ADLINK Technology, Inc. only supports the features and options listed in this manual. The main components used on the CoreModule 430 may provide more features or options than are listed in this manual. Some of these features/options are not supported on the module and will not function as specified in the chip documentation.
>
> Only the pinout tables of non-standard headers and connectors are included in this chapter. This chapter does not include pinout tables for standard headers and connectors such as PC/104, 44-pin IDE, and Compact Flash.

CPU

The CoreModule 430 offers two versions of an embedded microprocessor—the DMP Vortex 86SX and 86DX—operating at 300 and 800 MHz, respectively, combining a powerful x86 core and a selection of peripheral interfaces onto one chip. The 86SX and 86DX integrate CPU, Northbridge, and Southbridge functions. This single chip supports logic including PC/104, EIDE controllers and combines these with standard I/O interfaces to provide a PC compatible subsystem on a single chip.

Graphics

The CoreModule 430 provides a single PCI graphics controller chip which integrates a 2D engine and a PCI controller. The graphics controller incorporates a configurable 3.3V/2.5V DVO interface to support a third party TMDS transmitter and achieves high 2D performance with a DDR2 memory interface supporting a bandwith of up to 1 GB (DDR2 @ 250 MHz.)

Memory

The CoreModule 430 memory consists of the following element(s):

- System Memory
- Video Memory
- SPI Flash

System Memory

The CoreModule 430 provides two 16-bit, DDR2 memory chips of up to 128MB each for a total of up to 256MB of system memory soldered to the module and operating at 166MHz.

Video Memory

The CoreModule 430 provides one 16-bit, DDR2 memory chip of 32MB of video memory soldered to the module and operating at 166MHz.

SPI Flash

The CoreModule 430 features an on-board 16Mbit SPI Flash device, operating as a virtual Floppy Disk Drive. The board supports both the SPI Flash and an SPI header on the external SPI Bus. Enable the SPI Flash through the Boot screen of the BIOS Setup Utility. Refer to the Chapter 1 for a link to the SPI Flash data sheet.

Memory Map

The following table provides the common PC/AT memory allocations. These are DOS-level addresses. The OS typically hides these physical addresses by way of memory management. Memory below 000500h is used by the BIOS.

Table 3-1. Memory Map - Vortex 86SX/DX Processor

Base Address			Function
00000000h	-	0009FFFFh	Conventional Memory
000A0000h	-	000AFFFFh	Graphics Memory
000B0000h	-	000B7FFFh	Mono Text Memory
000B8000h	-	000BFFFFh	Color Text Memory
000C0000h	-	000C7FFFh	Standard Video BIOS
000D0000h	-	000DFFFFh	Reserved for Extended BIOS
000E0000h	-	000EFFFFh	Extended System BIOS Area
000F0000h	-	000FFFFFh	System BIOS Area (Storage and RAM Shadowing)
00100000h	-	Top of DRAM	Main DRAM Range
FFFC0000h [for SX processor] FFE00000h [for DX processor]	-	FFFFFFFFh	System Flash

Interrupt Channel Assignments

The interrupt channel assignments are shown in Table 3-2.

Table 3-2. Interrupt Channel Assignments

Device vs IRQ No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer	X															
Keyboard		X														
Secondary Cascade			X													
COM1					D											
COM2				D	O											
COM3				O	O						O	D				
COM4				O	O						D	O				
Parallel						O		D								
RTC									X							
IDE															D	
Math Coprocessor (only in DX processor)														X		
PS/2 Mouse													X			
PCI INTA	Automatically Assigned															
PCI INTB	Automatically Assigned															
PCI INTC	Automatically Assigned															
PCI INTD	Automatically Assigned															
USB	Automatically Assigned															
VGA	Automatically Assigned															
Ethernet	Automatically Assigned															

Legend: D = Default, O = Optional, X = Fixed

NOTE	The IRQs for the Ethernet, Video, and Internal Local Bus (ISA) are automatically assigned by the BIOS Plug and Play logic. Local IRQs assigned during initialization can not be used by external devices.

Table 3-3. DMA Map

DMA #	Use
0-1, 5, 6, 7	Direct Memory Access
3	LPT 1, only in ECP mode (configurable)
4	DMA 1 cascade

I/O Address Map

Table 3-4 shows the I/O address map. These are DOS-level addresses. The OS typically hides these physical addresses by way of memory management.

Table 3-4. I/O Address Map

Address (hex)	Subsystem
0000-000F	Primary DMA Controller (#1)
0020-0021	Master Interrupt Controller (#1)
0040-0043	Programmable Interrupt Timer (Clock/Timer)
0060	Keyboard Controller
0061	ISA Standard Port B
0063	ISA Standard Port B alias
0064	Keyboard Controller
0065	ISA Standard Port B alias
0067	ISA Standard Port B alias
0069	ISA Standard Port B alias
006B	ISA Standard Port B alias
006D	ISA Standard Port B alias
006F	ISA Standard Port B alias
0070-0071	RTC/ NMI enable
0080-008F	DMA Page
00A0-00A1	Slave Interrupt Controller (#2)
00C0-00DF	Secondary DMA Controller (#2)
00F0-00FF	Math Coprocessor (only in the DX processor)
01F0-01F7	IDE 0 (can be disabled)
02E8-2FF	Serial Port 4 (COM4) (base configuration @ 3F8h/2F8h/3E8h/**2E8h**/10)
02F8-02FF	Serial Port 2 (COM2) (base configuration @ 3F8h/**2F8h**/3E8h/2E8h/10)
0378-037F	LPT 1 (only in EPP modes, with default base address)
03E8-3EF	Serial Port 3 (COM3) (base configuration @ 3F8h/2F8h/**3E8h**/2E8h/10)
03F6	IDE 0 (see 1F0)
03F8-03FF	Serial Port 1 (COM1) (base configuration @ **3F8h**/2F8h/3E8h/2E8h/10)
0778-077A	LPT 1 (only in EPP modes, with default base address)
0CF8	PCI Configuration Address
0CFC-0CFF	PCI Configuration Data

Parallel Interface (LPT)

The Vortex x86 processor chip provides the Parallel Port interface. The Parallel Port supports the standard parallel, Bi-directional, Standard Printer Port (SPP), Enhanced Parallel Port (EPP), and Enhanced Capabilities Port (ECP) protocols.

Table 3-5 describes the pin signals of the Parallel interface, which uses a 26-pin, right-angle header with 2 rows, odd/even sequence (1, 2), and 0.079" (2mm) pitch.

Table 3-5. Parallel (LPT) Interface Pin/Signal Descriptions (J4)

Pin #	Signal	Description
1	Strobe*	Strobe* – This is an output signal used to strobe data into the printer. I/O pin in ECP/EPP mode.
2	AutoFD*	Auto Feed* – This is a request signal into the printer to automatically feed one line after each line is printed.
3	PD0	Parallel Port Data 0 – These pins (0 to 7) provides parallel port data signals.
4	ERR*	Error – This is a status output signal from the printer. A Low State indicates an error condition on the printer.
5	PD1	Parallel Port Data 1 – Refer to pin-3, PDO for more information.
6	INIT*	Initialize* – This signal is used to Initialize printer. Output in standard mode, I/O in ECP/EPP mode.
7	PD2	Parallel Port Data 2 – Refer to pin-3, PDO for more information.
8	SLIN	Select In – This output signal is used to select the printer. I/O pin in ECP/EPP mode.
9	PD3	Parallel Port Data 3 – Refer to pin-3, PDO for more information.
10	GND	Ground
11	PD4	Parallel Port Data 4 – Refer to pin-3, PDO for more information.
12	GND	Ground
13	PD5	Parallel Port Data 5 – Refer to pin-3, PDO for more information.
14	GND	Ground
15	PD6	Parallel Port Data 6 – Refer to pin-3, PDO for more information.
16	GND	Ground
17	PD7	Parallel Port Data 7 – Refer to pin-3, PDO for more information.
18	GND	Ground
19	Ack*	Acknowledge* – This is a status output signal from the printer. A Low State indicates it has received the data and is ready to accept new data.
20	GND	Ground
21	Busy*	Busy* – This is a Status output signal from the printer. A High State indicates the printer is not ready to accept data.
22	GND	Ground
23	PE	Paper End – This is a status output signal from the printer. A High State indicates it is out of paper.
24	GND	Ground
25	Slct	Select – This is a status output signal from the printer. A High State indicates it is selected and powered on.
26	Key/NC	Key Pin/Not Connected

Note: The shaded table cells denote power or ground. The * symbol indicates the signal is Active Low.

Serial Interface

The Vortex CPU contains the circuitry for all four serial ports. The CoreModule 430 provides serial ports 1 and 2 through transceivers U7 and U9 (headers J3 and J9), serial port 3 through transceiver U4 (header J14) and serial port 4 through transceiver U5 (header J13). The serial ports support the following features:

- Programmable word length, stop bits and parity
- 16-bit programmable baud rate generator
- Interrupt generator
- Loop-back mode
- 16-bit FIFOs for each port
- Ports 1, 2, 3, and 4 are supported by the Vortex processor and are 16C550/16C552 compatible
  - Serial 1 (J3, COM1) supports RS-232/RS-485 with full modem operation
  - Serial 2 (J9, COM2) supports RS-232/RS-485 with full modem operation
  - Serial 3 (J14, COM3) supports RS-232 with full modem operation
  - Serial 4 (J13, COM4) supports RS-232 with full modem operation

NOTE The RS-232/RS-485 mode for Serial Port 1 (COM1) and Serial Port 2 (COM2) are selected in BIOS Setup Utility. However, the RS-232 mode is the default (Standard) for any serial port.

RS-485 mode termination is selected with jumper JP2 Serial 1 (COM1) and JP1 Serial 2 (COM2) on the module. Refer to Table 2-3 for more information.

To implement the two-wire RS-485 mode on either serial port, you must tie the equivalent pins together for the selected port.

For example, you must tie pin 3 (Rx Data –) to 5 (Tx Data –) and pin 4 (Tx Data +) to 6 (Rx Data +) at Serial Port 1 or 2 (J3 or J9) for the two-wire interface. As an alternate, you may short the equivalent pins on the DB9 connector attached to respective serial port, as shown in Figure 3-1. Refer also to the following tables for the specific pins on the connectors. The RS-422 mode uses a four-wire interface and does not require combining pins for its operation, but you must select RS-485 in BIOS Setup.

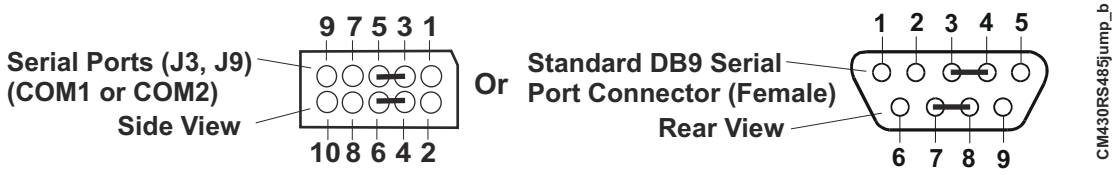

Figure 3-1. RS-485 Serial Port Implementation

Table 3-6 provides the signals for the corresponding pins of the two independent serial interfaces (Serial 1 & 2), and Table 3-7 provides the signals for the corresponding pins of two independent serial interfaces (Serial 3 & 4). Both interfaces use 10-pin, right-angle headers with 2 rows, odd/even sequence (1, 2), and 0.100" (2.54mm) pitch.

Table 3-6. Serial Ports 1 & 2 Interface Pin/Signal Descriptions (J3, J9)

Pin #	Signal	DB9 #	Description
1	DCD*	1	Data Carrier Detect – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR as part of the DTR/DSR handshake.
2	DSR*	6	Data Set Ready – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR for overall readiness.
3	RXD Rx Data –	2	Receive Data – Serial port receive data input is typically held at a logic 1 (mark) when no data is being transmitted, and is held "Off" for a brief interval after an "On" to "Off" transition on the RTS line to allow the transmission to complete. Serial Port 1 or 2 – If in RS-485 mode, this pin is Rx Data Negative.
4	RTS* Tx Data +	7	Request To Send – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS for low level flow control. Serial Port 1 or 2 – If in RS-485 mode, this pin is Tx Data Positive.
5	TXD Tx Data –	3	Transmit Data – Serial port transmit data output is typically held to a logic 1 when no data is being sent. Typically, a logic 0 (On) must be present on RTS, CTS, DSR, and DTR before data can be transmitted on this line. Serial Port 1 or 2 – If in RS-485 mode, this pin is Tx Data Negative.
6	CTS* Rx Data +	8	Clear To Send – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS for low level flow control. Serial Port 1 or 2 – If in RS-485 mode, this pin is Rx Data Positive.
7	DTR*	4	Data Terminal Ready – Indicates serial port is powered, initialized, and ready. Used as hardware handshake with DSR for overall readiness.
8	RI*	9	Ring Indicator – Indicates external serial device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
9	GND	5	Ground
10	Key/NC	NC	Key Pin/Not connected

Note: The shaded table cell denotes ground. The * symbol indicates the signal is Active Low.

Table 3-7. Serial Ports 3 & 4 Interface Pin/Signal Descriptions (J13, J14)

Pin #	Signal	DB9 #	Description
1	DCD*	1	Data Carrier Detect – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR as part of the DTR/DSR handshake.
2	DSR*	6	Data Set Ready – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR for overall readiness.
3	RXD	2	Receive Data – Serial port receive data input is typically held at a logic 1 (mark) when no data is being transmitted, and is held "Off" for a brief interval after an "On" to "Off" transition on the RTS line to allow the transmission to complete.

Table 3-7. Serial Ports 3 & 4 Interface Pin/Signal Descriptions (J13, J14) (Continued)

4	RTS*	7	Request To Send – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS for low level flow control.
5	TXD	3	Transmit Data – Serial port transmit data output is typically held to a logic 1 when no data is being sent. Typically, a logic 0 (On) must be present on RTS, CTS, DSR, and DTR before data can be transmitted on this line.
6	CTS*	8	Clear To Send – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS for low level flow control.
7	DTR*	4	Data Terminal Ready – Indicates serial port is powered, initialized, and ready. Used as hardware handshake with DSR for overall readiness.
8	RI*	9	Ring Indicator – Indicates external serial device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
9	GND	5	Ground
10	Key/NC	NC	Key Pin – Not connected

Note: The shaded table cell denotes ground. The * symbol indicates the signal is Active Low.

USB Interface

The CoreModule 430 contains one root USB (Universal Serial Bus) hub and two functional USB ports. The Vortex CPU provides the USB function including the following features:

- Provides one root hub with two USB ports
- Supports USB EHCI v.2.0 and USB OHCI v.1.1
- Provides over-current detection status
- Provides a fuse (F1, 1.5A) on board for over current protection

Table 3-8 describes the pin signals of the USB0 interface, which uses a single-row, 5-pin, right-angle header with 0.100" (2.54mm) pitch.

Table 3-8. USB0 Interface Pin/Signal Designations (J10)

Pin #	Signal	Description
1	USB0PWR	USB Power – VCC (+5V +/-5%) power goes to the port through an on board fuse. Port is disabled if this input is low.
2	USB0N	USB0 Port Data Negative
3	USB0P	USB0 Port Data Positive
4	GND	USB0 Port ground
5	SHIELD	USB0 Port shield

Note: The shaded table cells denote power or ground.

Table 3-9 describes the pin signals of the USB1 interface, which uses a single-row, 5-pin header with 0.079" (2mm) pitch.

Table 3-9. USB1 Interface Pin/Signal Designations (J17)

Pin #	Signal	Description
1	USB1PWR	USB Power – VCC (+5V +/-5%) power goes to the port through an on board fuse. Port is disabled if this input is low.
2	USB1N	USB1 Port Data Negative
3	USB1P	USB1 Port Data Positive

Table 3-9. USB1 Interface Pin/Signal Designations (J17) (Continued)

4	GND	USB1 Port ground
5	SHIELD	USB1 Port shield

Note: The shaded table cells denote power or ground.

Utility Interface

The Utility interface provides various utility and I/O signals on the module and consists of a 10-pin, 0.1" header. The Vortex CPU drives the signals on the Utility interface, and Table 3-10 provides the signal definitions.

- PS/2 Keyboard and Mouse
- Battery
- Reset Switch
- Speaker

Keyboard

The signal lines for a PS/2 keyboard are provided from the Vortex CPU to the Utility interface.

Mouse

The signal lines for a PS/2 mouse are provided from the Vortex CPU to the Utility interface.

Battery

An external battery input connection is provided through the Utility interface to support a battery backup for the CMOS RAM and the RTC (Real Time Clock).

Reset Switch

An external reset switch provides the reset signal through the Utility interface to a reset circuit, which drives the Vortex CPU.

Speaker

The speaker signal provides sufficient signal strength to drive a 1W 8 Ω “Beep” speaker through the Utility interface at an audible level. The speaker signal is driven from an on board amplifier and the Vortex CPU.

Table 3-10 describes the pin signals of the Utility interface, which uses a 10-pin, right-angle header with 2 rows, odd/even sequence (1, 2), and 0.100" (2.54mm) pitch.

Table 3-10. Utility Interface Pin/Signal Descriptions (J5)

Pin #	Signal	Description
1	SPKR	Speaker Output
2	BATV-	Ground return
3	RESETSW*	External Reset Switch signal
4	MDATA	Mouse Data input
5	KBDATA	Keyboard Data input
6	KBCLK	Keyboard Clock input
7	GND	Ground
8	KMPWR	Keyboard /Mouse power (+5V) output

Table 3-10. Utility Interface Pin/Signal Descriptions (J5) (Continued)

9	BATV+	Real time battery voltage (3.0V Max) input
10	MCLK	Mouse Clock input

Notes: The shaded table cells denote power or ground. The * symbol indicates the signal is Active Low.

Ethernet Interface

The Ethernet solution originates from the Vortex 86SX/DX CPU and consists of both the Media Access Controller (MAC) and the physical layer (PHY) combined into a single component solution. The Vortex Fast Ethernet Control Unit is a 32-bit PCI controller that features enhanced scatter-gather bus mastering capabilities, which enables the processor to perform high-speed data transfers over the internal PCI bus. The bus master capabilities enable the component to process high-level commands and perform multiple operations, thereby off-loading communication tasks from the CPU. The Ethernet interface offers the following features:

- Full duplex or half duplex support
- Full duplex support at 10 Mbps or 100 Mbps
- In full duplex mode, the Ethernet controller adheres to the IEEE 802.3x Flow Control specification.
- In half duplex mode, performance is enhanced by a proprietary collision reduction mechanism.
- IEEE 802.3 10/100BaseT compatible physical layer to wire transformer
- Two on board LEDs support the speed and the link & activity status
- IEEE 802.3u Auto-Negotiation support
- Fast back-to-back transmission support with minimum interframe spacing (IFS).
- IEEE 802.3x auto-negotiation support for speed and duplex operation
- 3 kB transmit and 3 kB receive FIFOs (helps prevent data underflow and overflow)
- IEEE 802.3x 100BaseTX flow control support
- On-board magnetics (Ethernet isolation transformer)

Table 3-11 describes the pin signals of the Ethernet interface, which uses a single-row, 8-pin header with 0.100" (2.54mm) pitch.

Table 3-11. Ethernet Interface Pin/Signal Descriptions (J2)

Pin #	Signal	Description
1	TX+	Analog Twisted Pair Ethernet Transmit Differential Pair – These pins transmit the serial bit stream through the isolation transformer.
2	TX-	
3	RX+	Analog Twisted Pair Ethernet Receive Differential Pair – These pins receive the serial bit stream through the isolation transformer.
6	RX-	
4	CT	Center Tap – Connected through two 75 ohm resistors in series to center tap of isolation transformer and then to ground through common 1k PF capacitor.
5	CT	
7	CT	Center Tap – Connected through two 75 ohm resistors in series to center tap of isolation transformer and then to ground through common 1k PF capacitor.
8	CT	

NOTE The magnetics (isolation transformer, U12) for the Ethernet connector is included on the CoreModule 430.

Video (TTL/VGA) Interface

The Volari Z9s graphics controller provides two graphics display ports for video signals to flat panel displays and traditional glass CRT monitors. The features are listed below:

- Enhanced 2D Graphics Controller
  - Full BitBLT Implementation for all 256 Raster Operations Defined for Windows
  - Supports 4 Transparent BLT Modes
    - Bitmap Transparency
    - Pattern Transparency
    - Source Transparency
    - Destination Transparency
  - Rectangle Clipping
  - Fast Line Draw Engine with styled pattern
  - Fast Rectangle Fill Engine
  - 256MB frame buffer with linear addressing
  - 64x64x2 bit-mapped mono hardware cursor
- VGA Output (DB15)
  - Supports 135 MHz triple RAMDACs for 1280 x 1024 x 75 Hz display
  - Supports 24-bit pixel depth
  - Supports interlaced or non-interlaced output
- TTL Output
  - Conforms with VESA Flat Panel Display Interface FPDI-1B
  - Supports up to 1600x1200 pixel display resolutions
  - Uses Internal CRT Controller for display modes settings
  - Supports 12-, 18-, and dual 12-bit Interface (1 pixel/clock)

Table 3-12 describes the pin signals of the Video interface, which uses a 44-pin, right-angle header with 2 rows, odd/even sequence (1, 2), and 0.079" (2mm) pitch.

Table 3-12. Video Interface Pin/Signal Descriptions (J11)

Pin #	Signal	Description
1	TFTDCLK	TFT Shift Clock – This clock signal provides the timing for transferring digital pixel data.
2	TFTDE	TFT Data Enable – This signal indicates valid data on any of the FP [23:0] lines.
3	TFTLP	TFT Line Pulse – This signal is the digital monitor equivalent of HSYNC.
4	TFTFrame	TFT Frame Marker – This signal is the TFT monitor equivalent of VSYNC.
5	GND	Ground
6	GND	Ground
7	NC	Not connected (FP0 = Panel Data 0)
8	NC	Not connected (FP1 = Panel Data 1)
9	FP2	Panel Data 2 – These pins (0 to 23) provides digital pixel data output signals.
10	FP3	Panel Data 3 – Refer to pin 9, FP2, for more information.
11	FP4	Panel Data 4 – Refer to pin 9, FP2, for more information.

Table 3-12. Video Interface Pin/Signal Descriptions (J11) (Continued)

12	FP5	Panel Data 5 – Refer to pin 9, FP2, for more information.
13	FP6	Panel Data 6 – Refer to pin 9, FP2, for more information.
14	FP7	Panel Data 7 – Refer to pin 9, FP2, for more information.
15	NC	Not connected (FP8 = Panel Data 8)
16	NC	Not connected (FP9 = Panel Data 9)
17	FP10	Panel Data 10 – Refer to pin 9, FP2, for more information.
18	FP11	Panel Data 11 – Refer to pin 9, FP2, for more information.
19	FP12	Panel Data 12 – Refer to pin 9, FP2, for more information.
20	FP13	Panel Data 13 – Refer to pin 9, FP2, for more information.
21	FP14	Panel Data 14 – Refer to pin 9, FP2, for more information.
22	FP15	Panel Data 15 – Refer to pin 9, FP2, for more information.
23	NC	Not connected (FP16 = Panel Data 16)
24	NC	Not connected (FP17 = Panel Data 17)
25	FP18	Panel Data 18 – Refer to pin 9, FP2, for more information.
26	FP19	Panel Data 19 – Refer to pin 9, FP2, for more information.
27	FP20	Panel Data 20 – Refer to pin 9, FP2, for more information.
28	FP21	Panel Data 21 – Refer to pin 9, FP2, for more information.
29	FP22	Panel Data 22 – Refer to pin 9, FP2, for more information.
30	FP23	Panel Data 23 – Refer to pin 9, FP2, for more information.
31	TFTEnVcc	TFT Power (Vcc) – This signal is the power to flat panel displays.
32	TFTEnVee	TFT Backlight Enable – This signal enables power to flat panel displays.
33	+PNLVdd	Voltage (+3.3 or +5 volts ±5%) depends on setting of JP6.
34	+12V Out	+12 volts ±5%
35	GND	Ground
36	GND	Ground
37	HSYNC	Horizontal Sync – This signal is used for the digital horizontal sync output to the CRT. Also used (with VSYNC) to signal power management state information to the CRT per the VESA™ DPMS™ standard.
38	VSYNC	Vertical Sync – This signal is used for the digital vertical sync output to the CRT. Also used (with HSYNC) to signal power management state information to the CRT per the VESA™ DPMS™ standard.
39	AGNDR	Analog Ground for Red
40	RED	Red – This pin provides the Red analog output to the CRT.
41	AGNDG	Analog Ground for Green
42	GREEN	Green – This pin provides the Green analog output to the CRT.
43	AGNDB	Analog Ground for Blue
44	BLUE	Blue – This pin provides the Blue analog output to the CRT.

Note: The shaded table cells denote power or ground. The * symbol indicates the signal is Active Low.

Serial Peripheral Interface (SPI)

The CoreModule 430 provides an SPI header for programming the SPI Flash virtual floppy drive.

Table 3-13 describes the pin signals of the SPI header, which provides a single-row of 6 pins with 0.079" (2mm) pitch.

Table 3-13. SPI Interface Pin/Signal Descriptions (J19)

Pin #	Signal	Description
1	EXT_CS*	SPI Chip Select
2	EXT_CLK	SPI Clock
3	EXT_DO	SPI Data Out
4	EXT_DI	SPI Data In
5	V.3.3	+3.3 Volts Power
6	GND	Ground

Note: The shaded table cells denote power or ground. The * symbol indicates the signal is Active Low.

Low Pin Count Interface (LPC)

The LPC interface provides expansion for custom LPC devices.

Table 3-14 describes the pin signals of the LPC interface, which uses a 10-pin header with 2 rows, odd/even sequence (1, 2), and 0.079" (2mm) pitch.

Table 3-14. LPC Interface Pin/Signal Descriptions (J20)

Pin #	Signal	Description
1	AD0	Command, Address, and Data 0
2	SERIRQ	Serial Interrupt Request
3	AD1	Command, Address, and Data 1
4	DRQ	DMA Request
5	AD2	Command, Address, and Data 2
6	FRAME	Frame Signals - indicate start of new cycle or termination of broken cycle
7	AD3	Command, Address, and Data 3
8	CLK_PCI	PCI Clock
9	V.3.3	+3.3 Volts Power
10	GND	Ground

Note: The shaded table cells denotes power or ground.

Miscellaneous

Real Time Clock (RTC)

The CoreModule 430 contains a Real Time (time of day) Clock (RTC), which can be backed up with an external cell battery. The CoreModule 430 will function without a battery in those environments which prohibit batteries. The CoreModule 430 will also continue to operate after the battery life has been exceeded. Under these conditions all setup information is restored from the on-board Flash memory during POST along with the default date and time information.

NOTE	Some operating systems require a valid default date and time to function.

User GPIO Interface

The CoreModule 430 provides GPIO pins for customer use, and the signals are routed to header J8. An example of how to use the GPIO pins resides in the Miscellaneous Source Code Examples on the CoreModule 430 Support Software QuickDrive.

The example program can be built by using the *make.bat* file. This produces a 16-bit DOS executable application, *gpio.exe*, which can be run on the CoreModule 430 to demonstrate the use of GPIO pins. For more information about the GPIO pin operation, refer to the Programming Manual for the Vortex processor at:

http://www.vortex86sx.com/

Table 3-12 describes the pin signals of the GPIO interface, which uses a 10-pin header with 2 rows, odd/even sequence (1, 2), and 0.079" (2mm) pitch.

Table 3-15. User GPIO Interface Pin/Signal Descriptions (J8)

Pin #	Signal	Description
1	GPIO0	User defined
2	GPIO1	User defined
3	GPIO2	User defined
4	GPIO3	User defined
5	GPIO4	User defined
6	GPIO5	User defined
7	GPIO6	User defined
8	GPIO7	User defined
9	GND	Ground
10	GND	Ground

Note: The shaded table cells denote ground.

Oops! Jumper (BIOS Recovery)

The Oops! jumper is provided in the event you have selected BIOS settings that prevent you from booting the system. By using the Oops! jumper you can stop the current BIOS settings in the CMOS from being loaded, allowing you to proceed, using the default settings. Connect the DTR pin to the RI pin on Serial port 1 (COM 1) prior to boot up to prevent the present BIOS settings from loading. After booting with the Oops! jumper in place, remove the Oops! jumper and go into the BIOS Setup Utility. Change the desired BIOS settings, or select the default settings, and save changes before rebooting the system.

To convert a standard DB9 connector to an Oops! jumper, short together the DTR (4) and RI (9) pins on the rear of the connector as shown in Figure 3-2 on the Serial Port 1 DB9 connector.

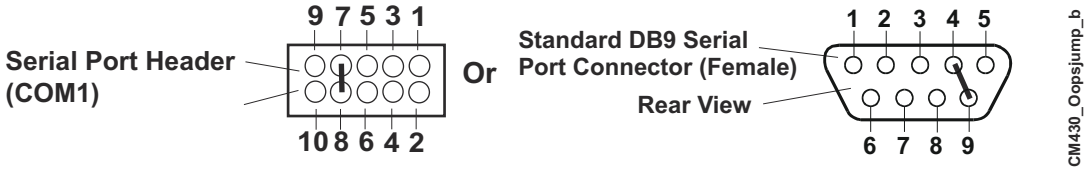

Figure 3-2. Oops! Jumper

Remote Access

The CoreModule 430 BIOS supports the remote access (or console redirection) feature. This I/O function is provided by an ANSI-compatible serial terminal, or the equivalent terminal emulation software running on another system. This can be very useful when setting up the BIOS on a production line for systems that are not connected to a keyboard and display.

Remote Access Setup

The remote access feature is implemented by connecting a standard null-modem cable or a modified serial cable (or "Hot Cable") between one of the serial ports, such as Serial 1 or 2 (J3 or J9), and the serial terminal or a PC with communications software. The BIOS Setup Utility controls the remote access settings on the CoreModule 430. Refer to Chapter 4, BIOS Setup for the settings of the remote access option, the serial terminal, or PC with communications software and the connection procedure.

Hot (Serial) Cable

To convert a standard serial cable to a Hot Cable, specific pins must be shorted together at the Serial port header or at the DB9 connector. Short together the RTS (4) and RI (8) pins on either serial port (J3 or J9) header. As an alternate, you can short the equivalent pins (pins 7 and 9) on the back of the respective DB9 port connector as shown in Figure 3-3.

Figure 3-3. Hot Cable Jumper

Watchdog Timer

The Watchdog Timer (WDT) restarts the system if an error or mishap occurs, allowing the system to recover from the mishap, even though the error condition may still exist. Possible problems include failure to boot properly, loss of control by the application software, failure of an interface device, unexpected conditions on the bus, or other hardware or software malfunctions.

The WDT (Watchdog Timer) can be used both during the boot process and during normal system operation.

- During the Boot process – If the OS fails to boot in the time interval set in the BIOS, the system will reset.

  Enable the *Watchdog Timer (sec)* field in the Chipset > Southbridge screen of BIOS Setup. Set the WDT for a time-out interval in seconds, between 1 and 255, in one second increments. Ensure you allow enough time for the operating system (OS) to boot. The OS or application must tickle (reset) the WDT before the timer expires. This can be done by accessing the hardware directly or through a BIOS call.

- During System Operation – An application can set up the WDT hardware through a BIOS call, or by accessing the hardware directly. Some ADLINK Board Support Packages provide an API to the WDT. The application must tickle (reset) the WDT before the timer expires or the system will be reset.

- Watchdog Code examples – ADLINK has provided source code examples on the CoreModule 430 Support Software QuickDrive illustrating how to control the WDT. The code examples can be easily copied to your development environment to compile and test the examples, or make any desired changes before compiling. Refer to the WDT Readme file in the Sample Code directory on the CoreModule 430 Support Software QuickDrive.

Power Interface

The CoreModule 430 requires one +5 volt DC power source. If the +5VDC power drops below ~4.65V, a low voltage reset is triggered, resetting the system.

The power input header (J7) supplies the following voltages and ground directly to the module:

- 5.0VDC +/- 5% @ 1.35 Amps

Table 3-16 describes the pin signals of the Power interface, which uses a 10-pin, right-angle header with 2 rows, odd/even sequence (1, 2), and 0.100" (2.54mm) pitch.

Table 3-16. Power Interface Pin/Signals (J7)

Pin	Signal	Descriptions
1	GND	Ground
2	+5V	+5 Volts
3	Key/GND	Key Pin on connector/Grounded on board
4	+12V	+12 volts routed to PC/104
5	GND	Ground
6	NC	Not connected
7	GND	Ground
8	+5V	+5 Volts
9	GND	Ground
10	+5V	+5 Volts

Note: The shaded table cells denote power or ground.

Chapter 4 BIOS Setup

Introduction

This chapter assumes the user is familiar with general BIOS Setup and does not attempt to describe the BIOS functions. Refer to "BIOS Setup Screens" on page 35 in this chapter for a map of the BIOS Setup settings. If ADLINK has added to or modified any of the standard BIOS functions, these functions will be described.

Entering BIOS Setup (Local Display)

To access BIOS Setup using a local display for the CoreModule 430:

1. Turn on the display and the power supply to the CoreModule 430.
2. Start Setup by pressing the [Del] key when the following message appears on the boot screen.

```
Press DEL to run Setup
```

> **NOTE** If the setting for *Quick Boot* is [Enabled], you may not see this prompt appear on screen. If this happens, press the <Del> key early in the boot sequence to enter BIOS Setup.

3. Follow the instructions on the right side of the screen to navigate through the selections and modify any settings.

Entering BIOS Setup (Remote Access)

This section describes how to enable the Remote Access in VGA mode and enter the BIOS setup through a serial terminal or PC.

1. Turn on the power supply to the CoreModule 430 and enter the BIOS Setup Utility in VGA mode.
2. Set the BIOS feature *Remote Access Configuration* to [Enable] under the **Advanced** menu.
3. Accept the default options or make your own selections for the balance of the Remote Access fields and record your settings.
4. Ensure you select the type of remote serial terminal you will be using and record your selection.
5. Select *Save Changes and Exit* and then shut down the CoreModule 430.
6. Connect the remote serial terminal (or the PC with communications software) to the COM port you selected and recorded earlier in the BIOS Setup Utility.
7. Turn on the remote serial terminal or PC and set it to the settings you selected in the BIOS Setup Utility.

   The default settings for the CoreModule 430 are:

   - COM1
   - 115200
   - 8 bits
   - 1 stop bit
   - no parity
   - no flow control
   - [Always] for *Redirection After BIOS POST*

8. Restore power to the CoreModule 430 and look for the screen prompt shown below.

   ```
   Press <space bar> to update BIOS
   ```

9. Press the F4 key to enter Setup (early in the boot sequence if *Quick Boot* is set to [Enabled].)

   If *Quick Boot* is set to [Enabled], you may never see the screen prompt.

10. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen.

> **NOTE** The serial console port is not hardware protected. Diagnostic software that probes hardware addresses may cause a loss or failure of the serial console functions.

OEM Logo Utility

The CoreModule 430 BIOS supports a graphical logo utility, which can be customized by the user and displayed when enabled through the BIOS Setup Utility. The graphical image can be a company logo or any custom image the user wants to display during the boot process. The custom image can be displayed as the first image displayed on screen during the boot process and remain there, depending on the options selected in BIOS Setup, while the OS boots.

Logo Image Requirements

The user's image may be customized with any image editing tool, and the system will automatically convert the image into an acceptable format to the tools (files and utilities) provided by ADLINK. The CoreModule 430 OEM Logo utility supports the following image formats:

- Bitmap image
  - 16-Color, 640x480 pixels
  - 256-Color, 640x480 pixels
- JPG image
  - 16-Color, 640x480 pixels
  - 256-Color, 800x600 pixels
  - 256-Color, 1024x768 pixels
- PCX image
  - 256-Color, 640x480 pixels
- A file size no larger than sample image

BIOS Setup Screens

This section provides illustrations of the seven main setup screens in the CoreModule 430 BIOS Setup Utility. Below each illustration is a bullet list of the screen's submenus and setting selections. The setting selections are presented in brackets after each submenu or menu item and the optimal default settings are presented in bold. For more detailed definitions of the BIOS settings, refer to the AMIBIOS8 manual: http://www.ami.com/support/doc/MAN-EZP-80.pdf

Table 4-1. BIOS Setup Menus

BIOS Setup Utility Menu	Item/Topic
Main Settings	Date and Time
Advanced Settings	CPU settings, IDE Drive Configurations, Remote Access (Serial Console), USB Configuration, and Southbridge LAN
PCIPnP (PCI, Plug n' Play)	PCI settings, Plug & Play settings, Interrupt settings and DMA channel settings, Reserved memory size
Boot	Boot-up Settings
Security	Setting or changing Passwords, Boot Sector Virus Protection
Chipset	Northbridge and Southbridge settings
Exit	Exiting with or without changing settings, Loading Optimal or Failsafe conditions

BIOS Main Setup Screen

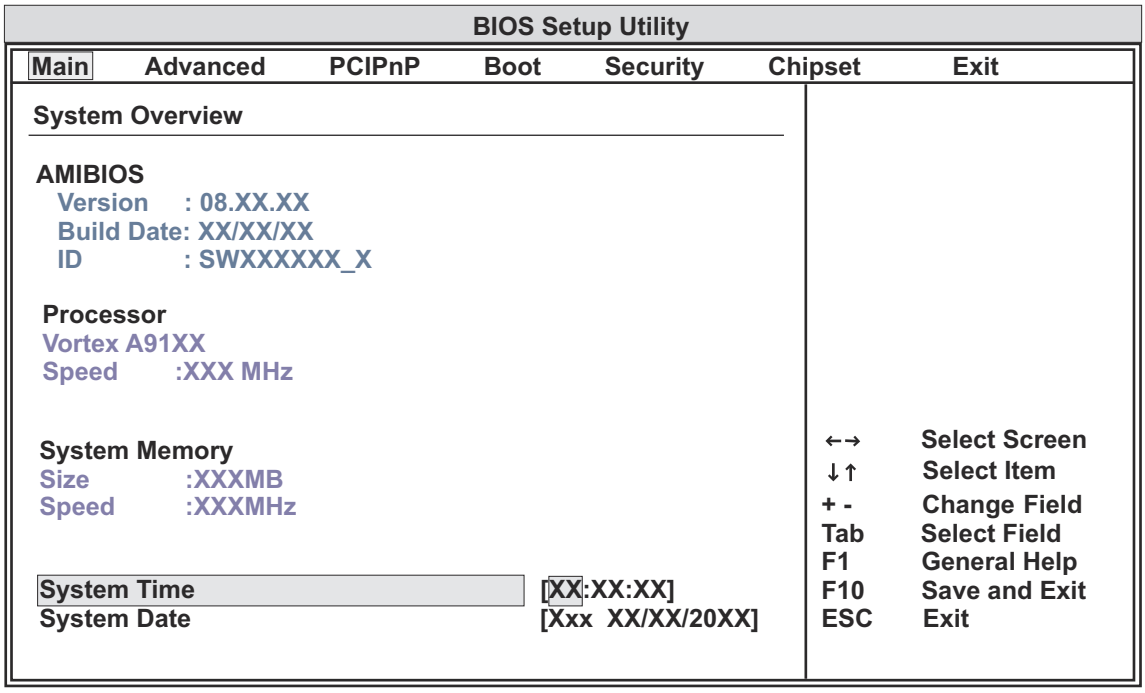

Figure 4-1. BIOS Main Setup Screen

- **Date & Time**
  - System Time (hh:mm:ss) – This is a 24-hour clock setting in hours, minutes, and seconds.

- System Date (day of week, mm:dd:yyyy) – This field requires the alpha-numeric entry of the day of week, day of the month, calendar month, and all 4 digits of the year, indicating the century plus year (*Fri 10/21/2011*).

BIOS Advanced Setup Screen

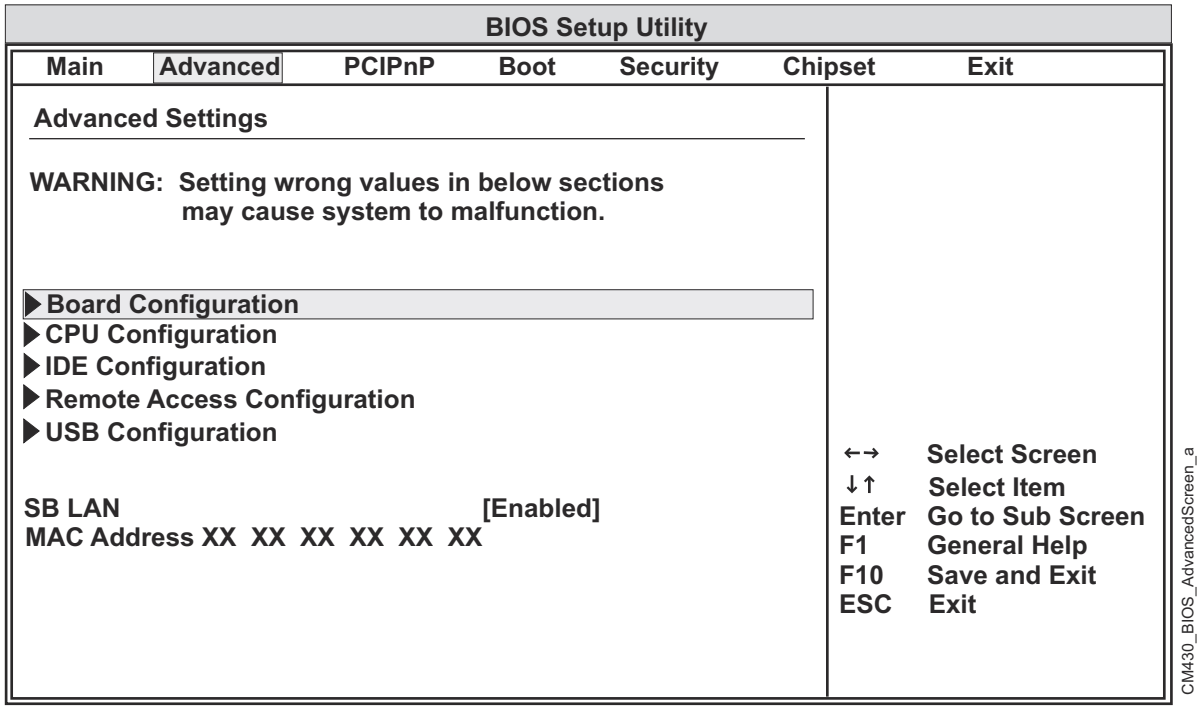

Figure 4-2. BIOS Advanced Setup Screen

Board Configuration

Chip Serial Number : XX XX XX XX XX XX

CPU Configuration

Manufacture:: DMP

Brand String:: Vortex A91XX

Frequency: : X00MHz

L1 Cache [Disabled; **Enabled**]

Cache L1 : XX KB

L2 Cache (only on DX model) [Disabled; **Enabled**]

Cache L2 : XXX KB

IDE Configuration

- OnBoard PCI IDE Controller – [Disabled; **Primary**; Secondary; Both]
  - Primary IDE Master : [Not Detected]
    - Type – [Not Installed; **Auto**; CD/DVD; ARMD]
    - LBA/Large Mode – [Disabled; **Auto**]
    - Block (Multi-Sector Transfer – [Disabled; **Auto**]

- PIO Mode – [**Auto**; 0; 1; 2; 3; 4]
- DMA Mode – [**Auto**]
- S.M.A.R.T. – [**Auto**; Disabled; Enabled]
- 32Bit Data Transfer – [Disabled; **Enabled**]

♦ Primary IDE Slave : [Not Detected]

- Type – [Not Installed; **Auto**; CD/DVD; ARMD]
- LBA/Large Mode – [Disabled; **Auto**]
- Block (Multi-Sector Transfer) – [Disabled; **Auto**]
- PIO Mode – [**Auto**; 0; 1; 2; 3; 4]
- DMA Mode – [**Auto**]
- S.M.A.R.T. – [**Auto**; Disabled; Enabled]
- 32Bit Data Transfer – [Disabled; **Enabled**]

♦ Secondary IDE Master : [Not Detected]

- Type – [**Not Installed**; Auto; CD/DVD; ARMD]

♦ Secondary IDE Slave : [Not Detected]

- Type – [**Not Installed**; Auto; CD/DVD; ARMD]

- Hard Disk drive Write Protect – [**Disabled**; Enabled]
- IDE Detect Time Out (Sec) – [0; 5; 10; 15; 20; 25; 30; **35**]
- ATA (PI) 80Pin Cable Detection – [**Host & Device**; Host; Device]
- Hard Disk Delay – [Disabled; 1 Second; **2 Second**; 4 Second; 8 Second]
- OnBoard IDE Operate Mode – [**Legacy Mode**; Native Mode]
- Not Program PIO mode – [**Disabled**; Primary Channel; Secondary Channel]
- Primary IDE Pin Select – [**Parallel IDE**; SD Card]

Remote Access Configuration

- Remote Access – [**Hotcable**; Enabled]
- Serial port number – [**COM1**; COM2]

  Base Address, IRQ [3F8h, 4]
- Serial Port Mode – [**115200 8, n, 1**; 57600 8, n, 1; 38400 8, n, 1; 19200 8, n, 1; 09600 8, n, 1]
- Flow Control – [**None**; Hardware; Software]
- Redirection After BIOS POST – [Disabled; Boot Loader; **Always**]
- Terminal Type – [**ANSI**; VT100; VT-UTF8]

  Note: If VT-UTF8 is selected, the following item disappears from the screen.
- VT-UTF8 Combo Key Support – [Disabled; **Enabled**]
- Sredir Memory Display Delay – [**No Delay**; Delay 1 sec; Delay 2 sec; Delay 4 sec]

USB Configuration

- USB Port 0, 1 – [**Enabled**; Disabled]
- USB Port 2, 3 – [**Enabled**; Disabled]
- USB Device – [**Enabled**; Disabled]

- Legacy USB Support – [Disabled; **Enabled**; Auto]

  Note: If Disabled is selected, the following item disappears from the screen.

- USB 2.0 Controller Mode – [Full Speed; **Hi Speed**]
- BIOS EHCI Hand-Off – [Disabled; **Enabled**]

SB LAN [**Enabled**; Disabled]

MAC Address **XX XX XX XX XX XX**

BIOS PCIPnP Setup Screen

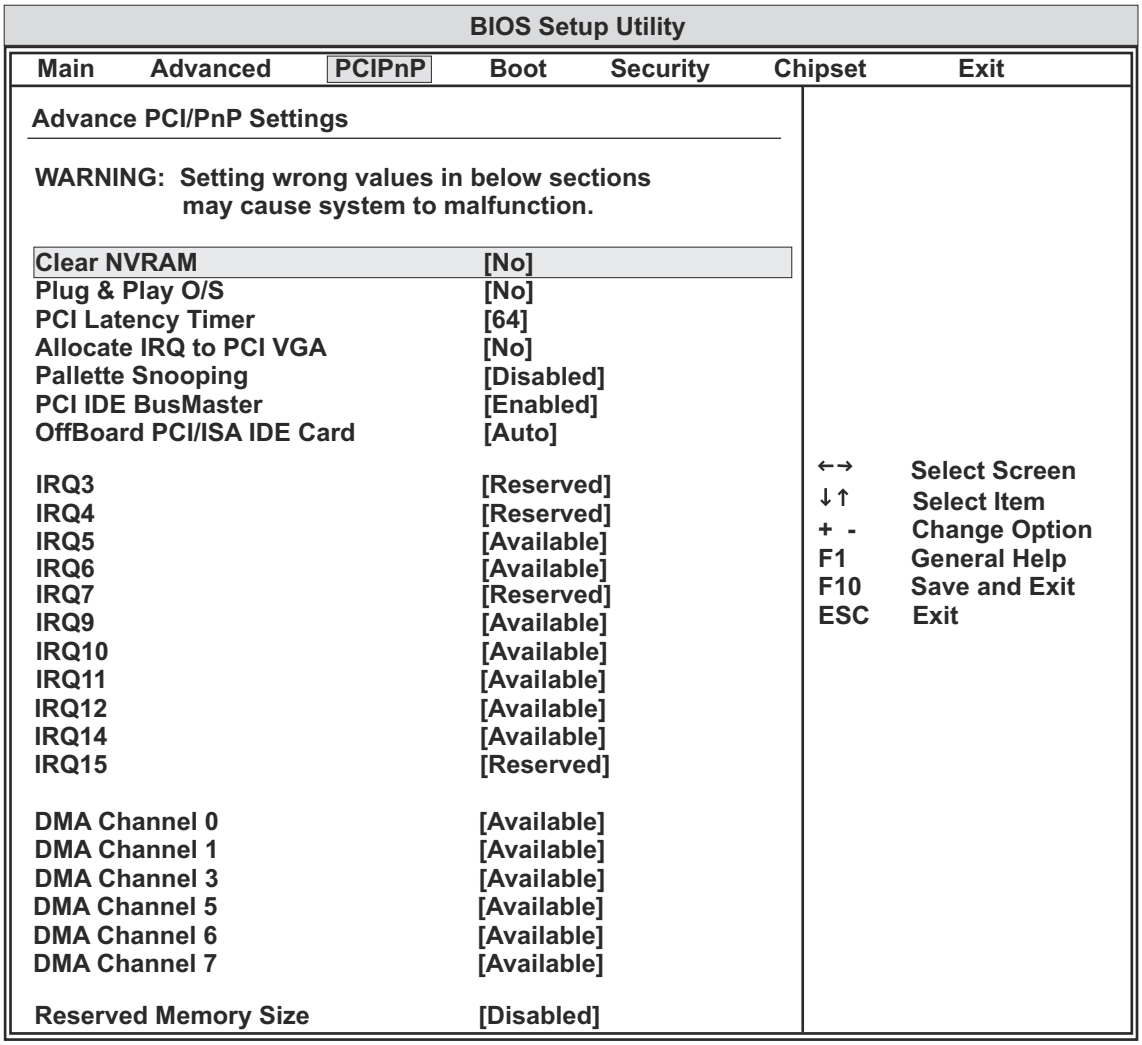

Figure 4-3. BIOS PCIPnP Setup Screen

- Clear NVRAM – [**No**; Yes]
- Plug & Play O/S – [**No**; Yes]
- PCI Latency timer – [32; **64**; 96; 128; 160; 192; 224; 248]
- Allocate IRQ to PCI VGA – [Yes; **No**]
- Palette Snooping – [**Disabled**; Enabled]

- PCI IDE BusMaster – [Disabled; **Enabled**]
- OffBoard PCI/ISA IDE card – [**Auto**; PCI Slot1; PCI Slot2; PCI Slot3; PCI Slot4; PCI Slot5; PCI Slot6]
- IRQ3 – [Available; **Reserved**]
- IRQ4 – [Available; **Reserved**]
- IRQ5 – [**Available**; Reserved]
- IRQ6 – [**Available**; Reserved]
- IRQ7 – [Available; **Reserved**]
- IRQ9 – [**Available**; Reserved]
- IRQ10 – [**Available**; Reserved]
- IRQ11 – [**Available**; Reserved]
- IRQ12 – [**Available**; Reserved]
- IRQ14 – [**Available**; Reserved]
- IRQ15 – [Available; **Reserved**]
- DMA Channel 0 – [**Available**; Reserved]
- DMA Channel 1 – [**Available**; Reserved]
- DMA Channel 3 – [**Available**; Reserved]
- DMA Channel 5 – [**Available**; Reserved]
- DMA Channel 6 – [**Available**; Reserved]
- DMA Channel 7 – [**Available**; Reserved]
- Reserved Memory – [**Disabled**; 16k; 32k; 64k]

BIOS Boot Setup Screen

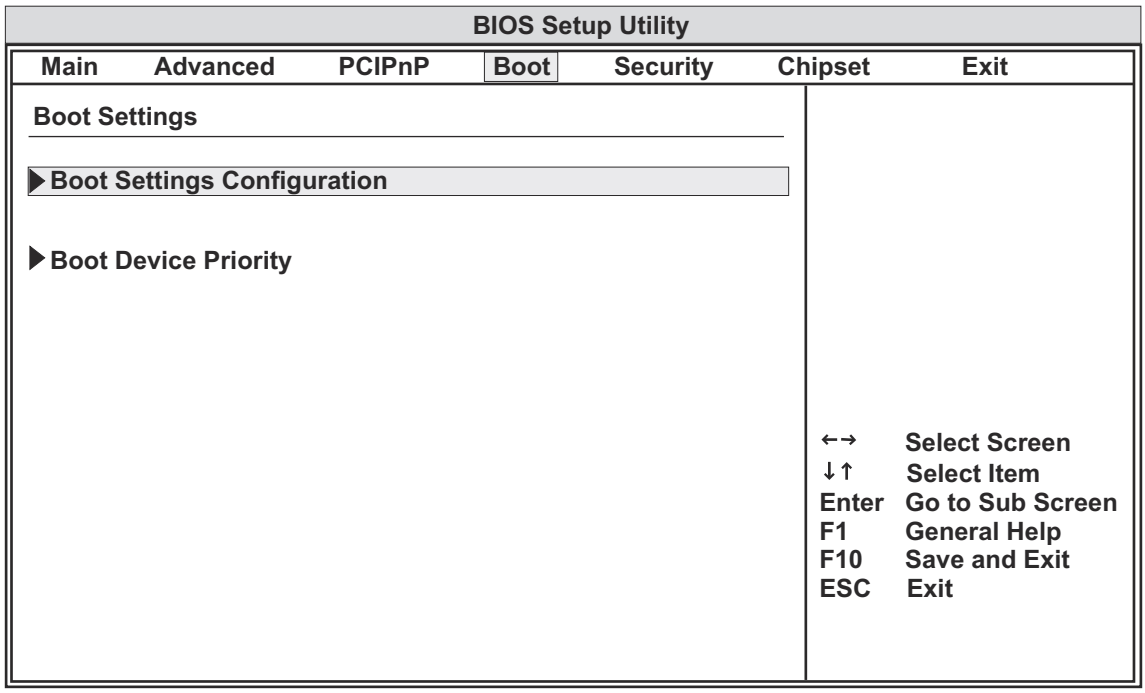

Figure 4-4. BIOS Boot Setup Screen

Boot Settings Configuration

- Quick Boot – [Disabled; **Enabled**]
- Quiet Boot – [**Disabled**; Enabled]
- Add On ROM Display Mode – [**Force BIOS**; Keep Current]
- Bootup Num-Lock – [**Off**; On]
- PS/2 Mouse Support – [Disabled; Enabled; **Auto**]
- Wait for 'F1' If Error – [**Disabled**; Enabled]
- Hit 'DEL' Message Display – [Disabled; **Enabled**]
- Interrupt 19 Capture – [Disabled; **Enabled**]
- Boot From LAN – [**Disabled**; Used INT 18h; Used INT 19h; PnP/BEV (BBS); RPL]
- Beep Function – [**Disabled**; Enabled]
- OnBoard Virtual Flash FDD – [**Disabled**; Enabled; Diskette Write Protect]

BIOS Security Setup Screen

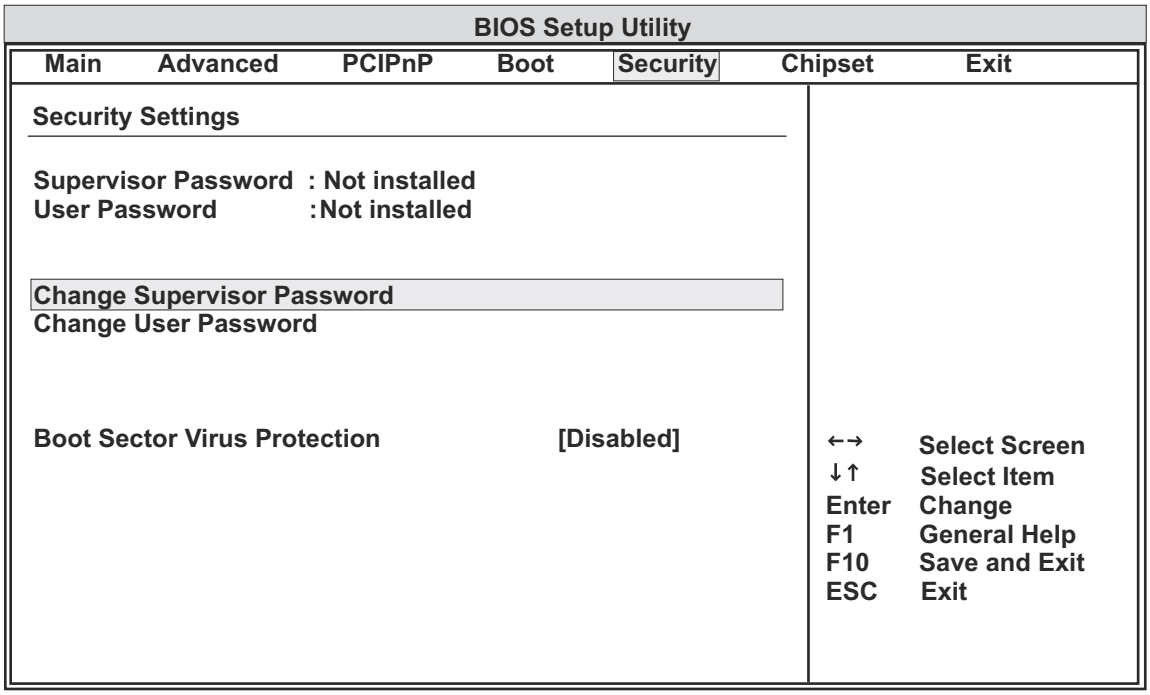

Figure 4-5. BIOS Security Setup Screen

- Supervisor Password – [**Not Installed**]
- User Password – [**Not Installed**]
- Change Supervisor Password
  a. Select *Change Supervisor Password* from the Security Setup menu.
  b. Press <*Enter*> to access the pop-up entry field, *Enter New Password.*
  c. Type the password and press <*Enter*> again.
     The screen will not display the password as you type.
  d. Re-type the password when prompted by the pop-up entry field and press <*Enter*> again.
     If the password is not confirmed when you re-type it, an error message will appear. The password is stored in NVRAM if you have successfully entered the password.
- Change User Password
  a. Select *Change User Password* from the Security Setup menu.
  b. Press <*Enter*> to access the pop-up entry field, *Enter New Password.*
  c. Type the password and press <*Enter*> again.
     The screen will not display the password as you type.
  d. Re-type the password when prompted by the pop-up entry field and press <*Enter*> again.
     If the password is not confirmed when you re-type it, an error message will appear. The password is stored in NVRAM if you have successfully entered the password.
- Boot Sector Virus Protection – [**Disabled**; Enabled]

BIOS Chipset Setup Screen

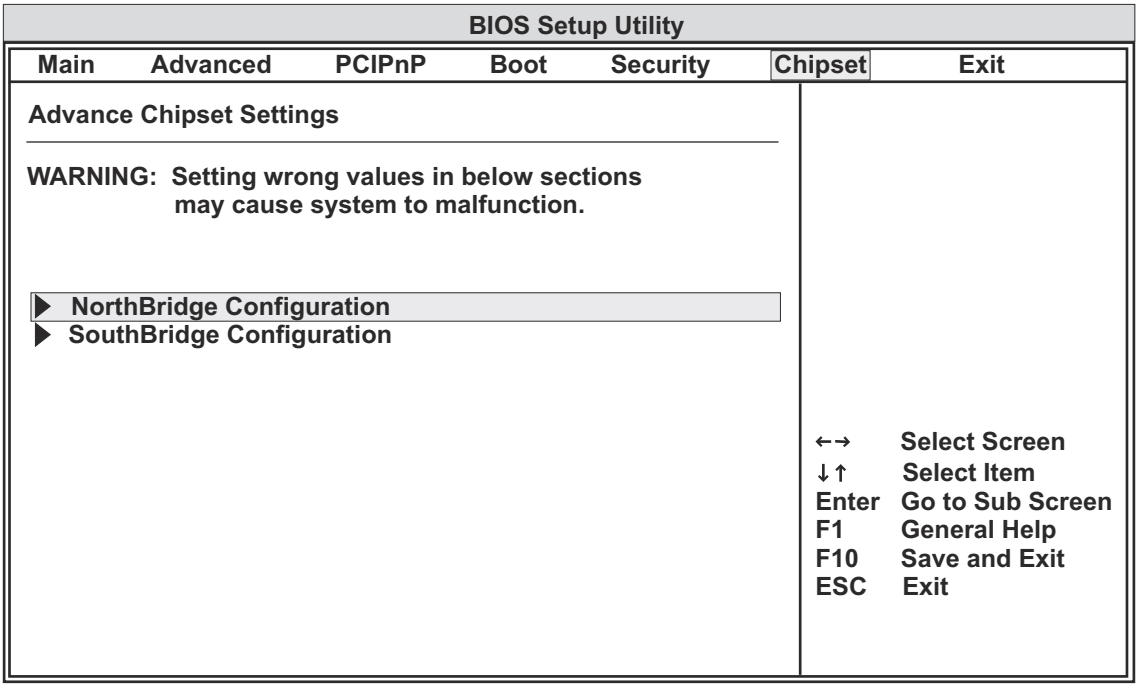

Figure 4-6. BIOS Chipset Setup Screen

NorthBridge Configuration

- NorthBridge Chipset Configuration
  - DRAM Timing Setting By – [BIOS]
  - CPU Speed Setting By – [**Divide By 1**; Divide By 2; Divide By 3; Divide By 4; Divide By 5; Divide By 6; Divide By 7; Divide By 8]

SouthBridge Configuration

- SouthBridge Chipset Configuration

  P.O.S.T. Forward To [**Disabled**; COM1]
  - ISA Configuration
    - ISA Clock – [**8.3MHz**; 16.6MHz]
    - ISA 16bits I/O wait-state – [**1 clock**; 2 clock; 3 clock; 4 clock; 5 clock; 6 clock; 7 clock; 8 clock]

- ISA 8bits I/O wait-state – [1 clock;
  2 clock;
  3 clock;
  4 clock;
  5 clock;
  6 clock;
  7 clock;
  8 clock]
- ISA 16bits Memory wait-state – [0 clock;
  1 clock;
  2 clock;
  3 clock;
  4 clock;
  5 clock;
  6 clock;
  7 clock]
- ISA 8bits Memory wait-state – [1 clock;
  2 clock;
  3 clock;
  4 clock;
  5 clock;
  6 clock;
  7 clock;
  8 clock]

♦ Serial Port Configuration

- SB Serial Port 1 – [Disabled; **3F8**; 2F8; 3E8; 2E8; 10]
  - Serial Port IRQ 1 [IRQ3; **IRQ4**; IRQ9; IRQ10; IRQ11]
  - Serial Port Baud Rate [2400 BPS; 4800 BPS; 9600 BPS; 19200 BPS; 38400 BPS; 57600 BPS; **115200 BPS**]
  - Serial Port Type [**RS232**; RS485]
- SB Serial Port 2 – [Disabled; 3F8; **2F8**; 3E8; 2E8; 10]
  - Serial Port IRQ 2 [**IRQ3**; IRQ4; IRQ9; IRQ10; IRQ11]
  - Serial Port Baud Rate [2400 BPS; 4800 BPS; 9600 BPS; 19200 BPS; 38400 BPS; 57600 BPS; **115200 BPS**]
  - Serial Port Type [**RS232**; RS485]
- SB Serial Port 3 – [**Disabled**; 3F8; 2F8; 3E8; 2E8; 10]
- SB Serial Port 4 – [**Disabled**; 3F8; 2F8; 3E8; 2E8; 10]

♦ WatchDog Configuration

- WatchDog 0 Function – [Enabled; **Disabled**]
- WatchDog 1 Function – [Enabled; **Disabled**]

♦ Multi-Function Port Configuration

- Port0 Function – [**GPIO**; 8051 P0; PWM00 . . PWM07]
- Port0 Bit0 Direction – [**IN**; OUT]
- Port0 Bit1 Direction – [**IN**; OUT]
- Port0 Bit2 Direction – [**IN**; OUT]
- Port0 Bit3 Direction – [**IN**; OUT]
- Port0 Bit4 Direction – [**IN**; OUT]
- Port0 Bit5 Direction – [**IN**; OUT]

- Port0 Bit6 Direction – [**IN**; OUT]
- Port0 Bit7 Direction – [**IN**; OUT]
- Port1 Function – [**GPIO**; PWM16. .PWM23]
- Port1 Bit2 Direction – [**IN**; OUT]
- Port1 Bit3 Direction – [**IN**; OUT]
- Port1 Bit4 Direction – [**IN**; OUT]
- Port1 Bit5 Direction – [**IN**; OUT]
- Port1 Bit6 Direction – [**IN**; OUT]
- Port1 Bit7 Direction – [**IN**; OUT]

- Port2 Function – [**GPIO**; 8051 P2; PWM16. .PWM23]
- Port2 Bit0 Direction – [**IN**; OUT]
- Port2 Bit1 Direction – [**IN**; OUT]
- Port2 Bit2 Direction – [**IN**; OUT]
- Port2 Bit3 Direction – [**IN**; OUT]
- Port2 Bit4 Direction – [**IN**; OUT]
- Port2 Bit5 Direction – [**IN**; OUT]
- Port2 Bit6 Direction – [**IN**; OUT]
- Port2 Bit7 Direction – [**IN**; OUT]

- Port3 Bit0 Function – [**GPIO**; 8051 P3; SPI]
  - Direction – [**IN**; OUT]
- Port3 Bit1 Function – [**GPIO**]
  - Direction – [**IN**; OUT]
- Port3 Bit2 Function – [**GPIO**]
  - Direction – [**IN**; OUT]
- Port3 Bit3 Function – [**GPIO**]
  - Direction – [**IN**; OUT]

- Port3 Bit4 Function – [**GPIO**; I2C]
  - Direction – [**IN**; OUT]
- Port3 Bit5 Function – [**GPIO**]
  - Direction – [**IN**; OUT]

- Port3 Bit6 Function – [**GPIO**; I2C]
  - Direction – [**IN**; OUT]
- Port3 Bit7 Function – [**GPIO**]
  - Direction – [**IN**; OUT]

- GPCS Configuration
  - GPCS0 Function – [Enabled; **Disabled**]
  - GPCS1 Function – [Enabled; **Disabled**]
- Redundancy Control Configuration
  - Dual Port 4 KB SRAM – [Enabled; **Disabled**]
  - SB Serial Port 9 – [**Disabled**; 3F8; 2F8; 3E8; 2E8; 10]
  - WatchDog0 Condition – [**Disabled**; Enabled]
  - WatchDog1 Condition – [**Disabled**; Enabled]
  - Invalid OPCODE Condition – [**Disabled**; Enabled]
  - KB/MS System Fail – [**Normal**; TRI-State]
  - GPIO PORT0 System Fail – [**Normal**; TRI-State]
  - GPIO PORT1 System Fail – [**Normal**; TRI-State]
  - GPIO PORT2 System Fail – [**Normal**; TRI-State]
  - UART1 System Fail – [**Normal**; TRI-State]
  - UART2 System Fail – [**Normal**; TRI-State]
  - UART3 System Fail – [**Normal**; TRI-State]
  - UART4 System Fail – [**Normal**; TRI-State]

BIOS Exit Setup Screen

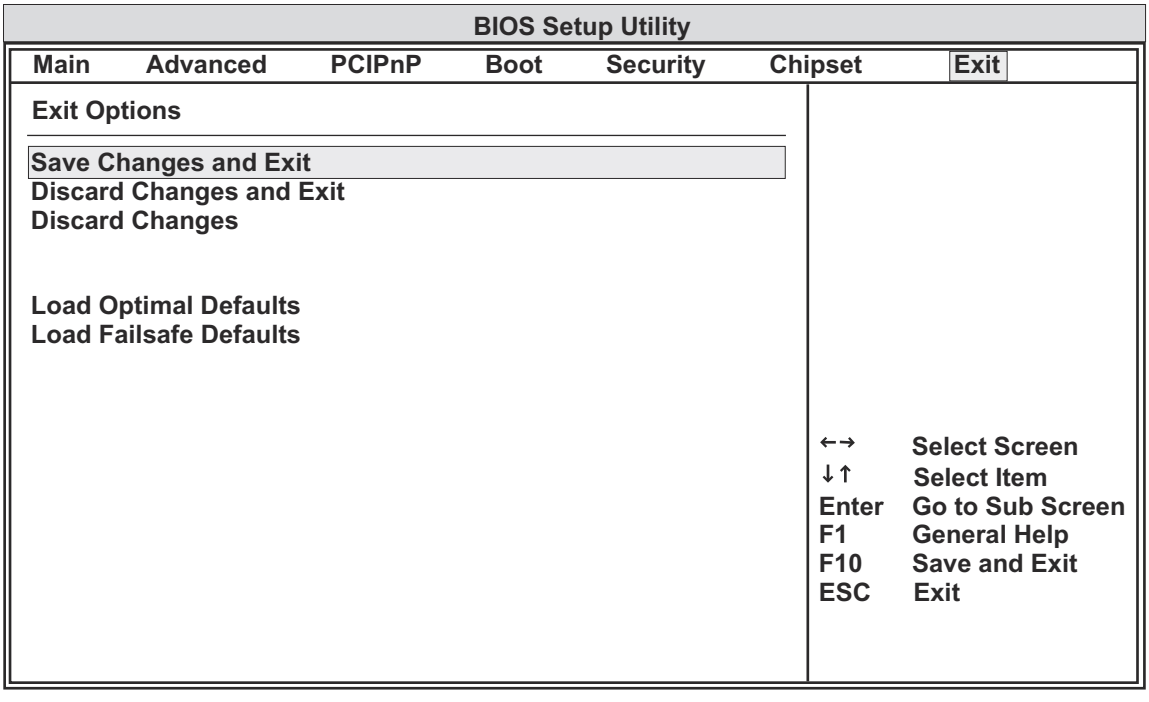

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Figure 4-7. BIOS Exit Setup Screen

Save Changes and Exit

The < F10 > key can be used for this operation.

Discard Changes and Exit

The < ESC > key can be used for this operation.

Discard Changes

The < F7 > key can be used for this operation.

Load Optimal Defaults

The < F9 > key can be used for this operation.

Load Failsafe Defaults

The < F8 > key can be used for this operation.

Appendix A Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed in the Table A-1 below. Requests for support through the Ask an Expert are given the highest priority, and usually will be addressed within one working day.

- ADLINK Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the Ampro By ADLINK web page at http://www.adlinktech.com/AAE/. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.

  ADLINK strongly suggests that you register with the web site. By creating a profile on the ADLINK web site, you will have a portal page called "My ADLINK" unique to you with access to exclusive services and account information.

- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to the My Question area where you can check status, update your request, and access other features.

- Download Service – This service is also free and available 24 hours a day at http://www.adlinktech.com. For certain downloads such as technical documents and software, you must register online before you can log in to this service.

Table A-1. Technical Support Contact Information

Method	Contact Information
Ask an Expert	http://www.adlinktech.com/AAE/
Web Site	http://www.adlinktech.com
Standard Mail	Contact us should you require any service or assistance. **ADLINK Technology, Inc.** Address: 9F, No.166 Jian Yi Road, Zhonghe District New Taipei City 235, Taiwan 新北市中和區建一路 166 號 9 樓 Tel: +886-2-8226-5877 Fax: +886-2-8226-5717 Email: service@adlinktech.com **Ampro ADLINK Technology, Inc.** Address: 5215 Hellyer Avenue, #110, San Jose, CA 95138, USA Tel: +1-408-360-0200 Toll Free: +1-800-966-5200 (USA only) Fax: +1-408-360-0222 Email: info@adlinktech.com **ADLINK Technology (China) Co., Ltd.** Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203) 300 Fang Chun Rd., Zhangjiang Hi-Tech Park, Pudong New Area, Shanghai, 201203 China Tel: +86-21-5132-8988 Fax: +86-21-5132-3588 Email: market@adlinktech.com

Table A-1. Technical Support Contact Information (Continued)

	ADLINK Technology Beijing Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室(100085) Rm. 801, Power Creative E, No. 1, B/D Shang Di East Rd., Beijing, 100085 China Tel: +86-10-5885-8666 Fax: +86-10-5885-8625 Email: market@adlinktech.com **ADLINK Technology Shenzhen** Address: 深圳市南山区科技园南区高新南七道 数字技术园 A1 栋 2 楼 C 区 (518057) 2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7, High-Tech Industrial Park S., Shenzhen, 518054 China Tel: +86-755-2643-4858 Fax: +86-755-2664-6353 Email: market@adlinktech.com **ADLINK Technology (Europe) GmbH** Address: Nord Carree 3, 40477 Duesseldorf, Germany Tel: +49-211-495-5552 Fax: +49-211-495-5557 Email: emea@adlinktech.com **ADLINK Technology, Inc. (French Liaison Office)** Address: 15 rue Emile Baudot, 91300 Massy CEDEX, France Tel: +33 (0) 1 60 12 35 66 Fax: +33 (0) 1 60 12 35 66 Email: france@adlinktech.com **ADLINK Technology Japan Corporation** Address: 〒101-0045 東京都千代田区神田鍛冶町 3-7-4 神田 374 ビル 4F KANDA374 Bldg. 4F, 3-7-4 Kanda Kajicho, Chiyoda-ku, Tokyo 101-0045, Japan Tel: +81-3-4455-3722 Fax: +81-3-5209-6013 Email: japan@adlinktech.com **ADLINK Technology, Inc. (Korean Liaison Office)** Address: 서울시 서초구 서초동 1506-25 한도 B/D 2 층 2F, Hando B/D, 1506-25, Seocho-Dong, Seocho-Gu, Seoul 137-070, Korea Tel: +82-2-2057-0565 Fax: +82-2-2057-0563 Email: korea@adlinktech.com **ADLINK Technology Singapore Pte. Ltd.** Address: 84 Genting Lane #07-02A, Cityneon Design Centre, Singapore 349584 Tel: +65-6844-2261 Fax: +65-6844-2263 Email: singapore@adlinktech.com **ADLINK Technology Singapore Pte. Ltd. (Indian Liaison Office)** Address: No. 1357, "Anupama", Sri Aurobindo Marg, 9th Cross, JP Nagar Phase I, Bangalore - 560078, India Tel: +91-80-65605817 Fax: +91-80-22443548 Email: india@adlinktech.com

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